Programmer's reference manual for a digital CRT display

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PROGRAMMER'S REFERENCE MANUAL FOR A DIGITAL CRT DISPLAY

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ABSTRACT

Command and data formats for a digital cathode-ray tube display are described. The display is used with a small digital computer as a testing ground for developments in hardware and software relating to man-machine communications problems. The information contained in this manual is sufficient to allow the user to write and to understand machine language display programs.

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PROGRAMMER'S REFERENCE MANUAL FOR A DIGITAL CRT DISPLAY

- J.K. Pulfer -

INTRODUCTION

The cathode-ray tube digital display, which is used with a small computer*, is primarily a research tool for both hardware and software development. At times it is also used as a communication device between the system executive and the operator or user. Because the display is used to test hardware ideas, its internal circuitry is continuously undergoing modification. It follows that any programmer's reference guide will be obsolete as soon as it is written. Nevertheless, there appears to be a need to collect in one location much of the information necessary to write display programs, and this report has been prepared to meet that need.

HARDWARE DESCRIPTION

The CRT display together with its buffer core memory can be described as a special purpose computer capable of storing a wide variety of commands and data words and of executing the commands in either an on-line or off-line mode. In addition, a number of input devices are available through which analog and digital information supplied by an operator can be transmitted to the display and, if desired, forwarded to the computer.

Figure 1 is a simplified block diagram of some of the hardware elements in the processing system at the present time (March 1968). Figure 2 shows in more detail those elements which are part of the display system.

Data are transferred between computer, display, and keyboard in the form of 24-bit words, and between the buffer memory and display as 26-bit words.

24-bit computer words are interpreted by the display either as data words, or as command words.

A word may be recognized as a command word for one of three reasons:

1) It was produced by the execution of a CEU command in the computer CPU and is therefore accompanied by a command strobe at the interface between the display and the computer input/output bus.

2) It was produced by reading a word from the external core buffer in which the twenty-fifth bit in the word was set to a binary 1.

3) It was immediately preceded by a data word in which all 24 bits were zero (25 in the case of buffer memory). All other words will be interpreted as data words.

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* Systems Engineering Laboratories Model 840A

Command words are stored in the display command register (C register).

Data words are stored in the display data register (D register) and transferred to various other places in the display according to the current word in the command register. That is to say, the 24-bit data word is interpreted by the display according to the current word in the C register. The remainder of this guide will be used to define the various types of command word, and to show the resulting data word format which accompanies them.

There are also a number of command words which are interpreted only by the buffer memory and are, therefore, meaningless if transferred from the computer CPU to the C register.

DISPLAY COMMANDS

Instruction Format

1) Immediate, or real-time execution (direct from computer CPU to C register).
The mnemonic form of the instruction is:

```
CEU '40, W
DATA 'XBCDEFGH
```

where the Wait flag in the CEU instruction is optional.

'XBCDEFGH represents an 8-digit octal number defining the command. The functions of the various digits will be outlined below.

X must be zero.

2) Stored, or delayed execution (transferred from the computer CPU to the 4K buffer memory for later use).

```
CEU '41,W
DATA 'XBCDEFGH
```

where 'XBCDEFGH is an 8-digit octal number.

X must be zero.

3) Implied display command (following an all-zero data word).

```
DATA 'XBCDEFGH
```

where XBCDEFGH is an 8-digit octal number.

X must be zero.

4) Memory command word (a word which is interpreted only by the buffer memory and has no meaning to the display).

```
CEU '41,W
DATA 'XBCDEFGH
```

where X may not be zero.

DISPLAY COMMAND WORD FORMATS

Figure 3 is a block diagram of a portion of the display control unit showing some of the registers used in executing a display command. As outlined above, the word stored in the C register may be expressed as an 8-digit octal number 'XBCDEFGH.

The following examples describe the display behaviour for individual portions of the command word. An actual command may be made up of a number of these micro commands, and all will be executed simultaneously. There are, of course, some impossible or meaningless combinations.

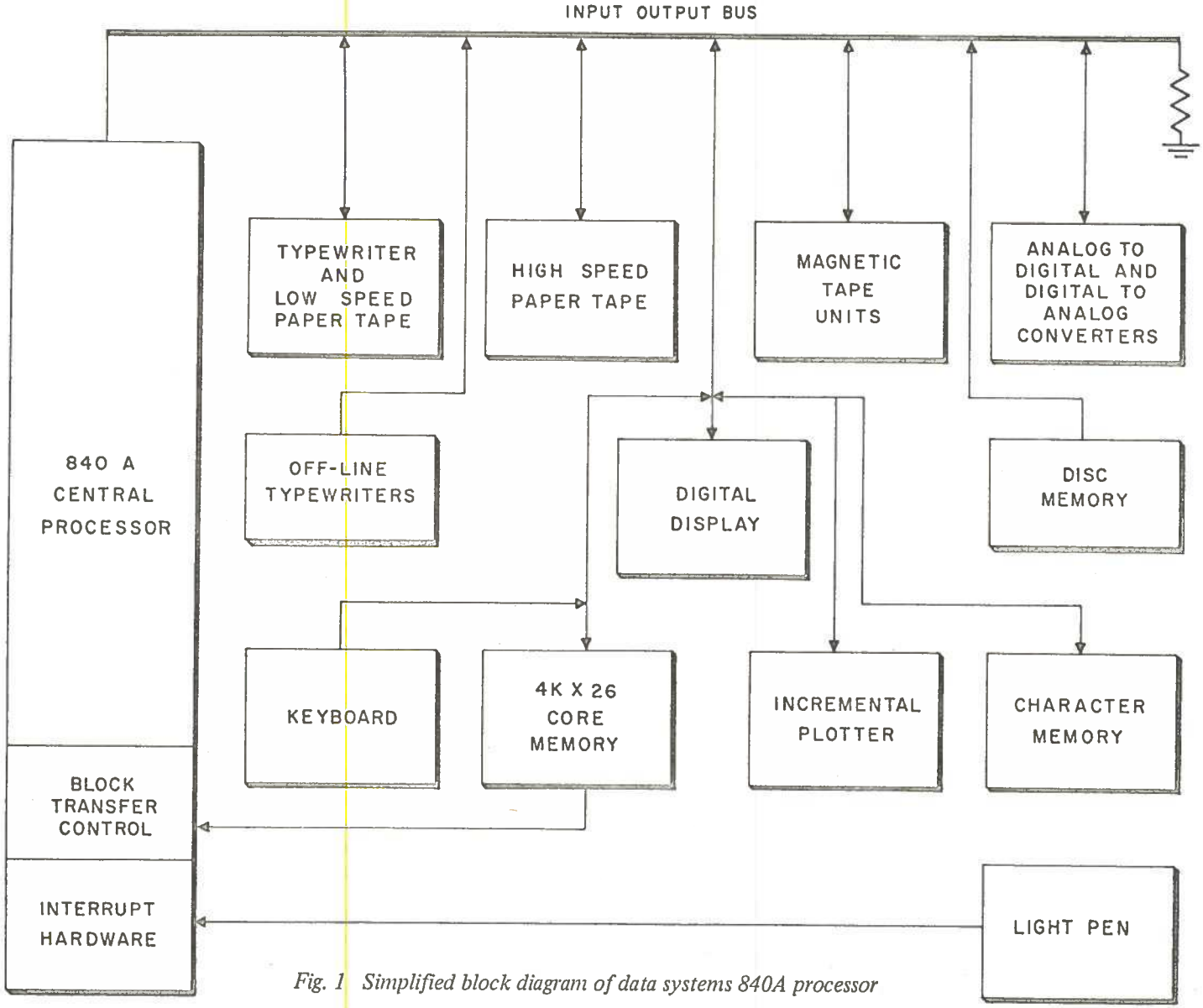


Fig. 1 Simplified block diagram of data systems 840A processor

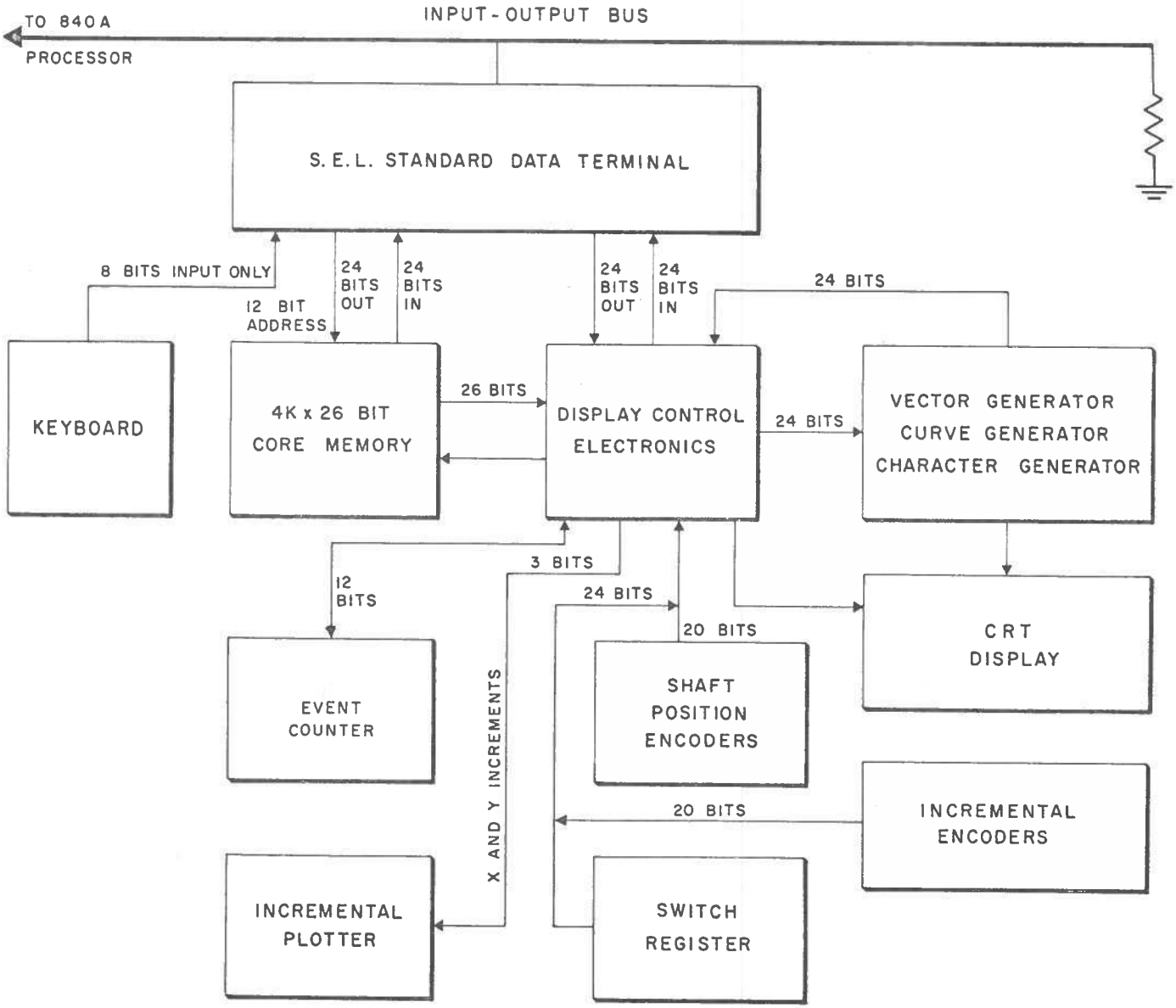


Fig. 2 Block diagram of electronics connected to display data terminal

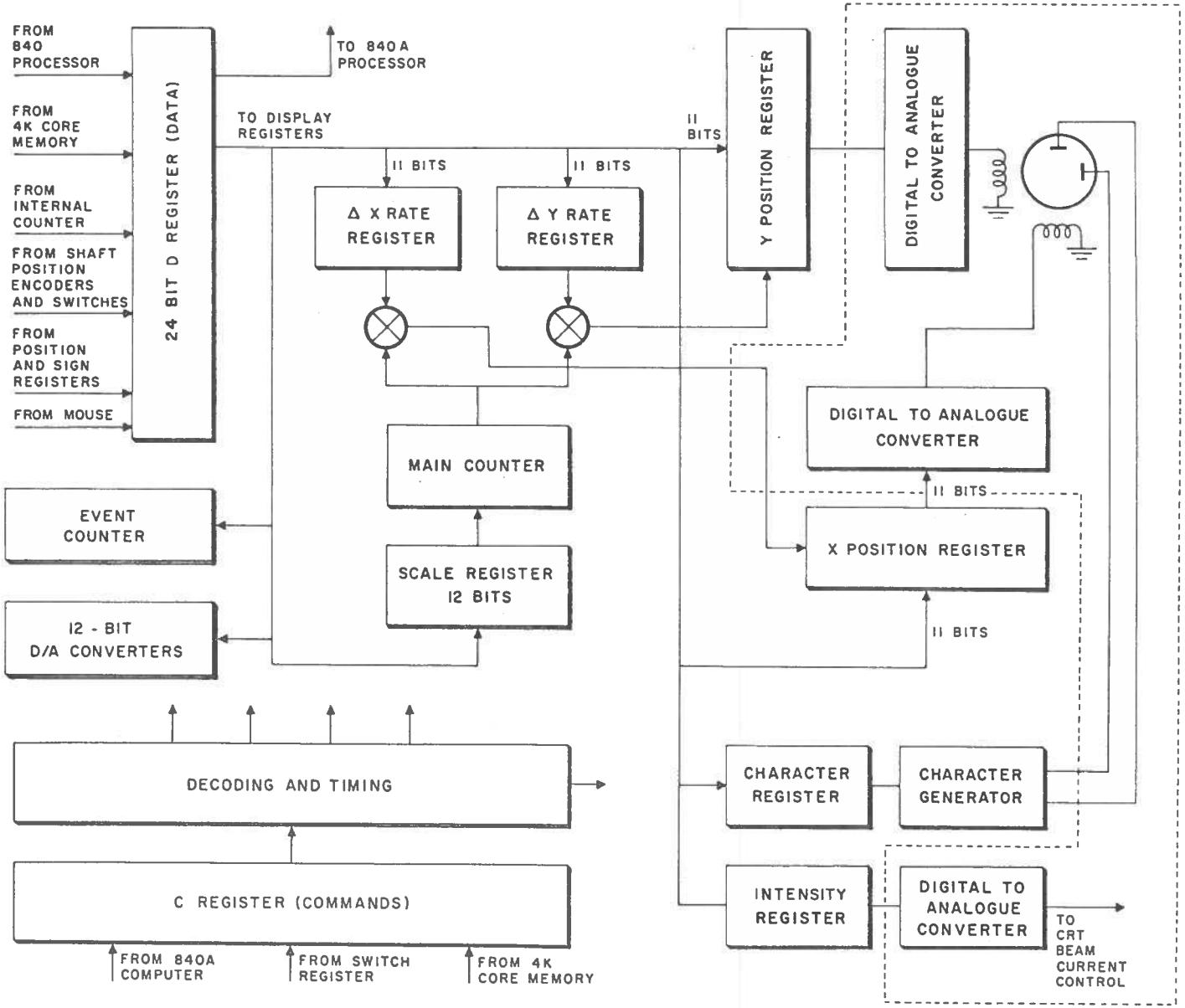


Fig. 3 Simplified display control electronics

X			B			C			D			E			F			G			H		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *NO-OP – no function performed*

TIMING: ≈ 9 μsec from CPU
≈ 2 μsec from buffer

ASSOCIATED DATA FORMAT:

NONE

NOTES:

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *TRANSFER ZEROS*

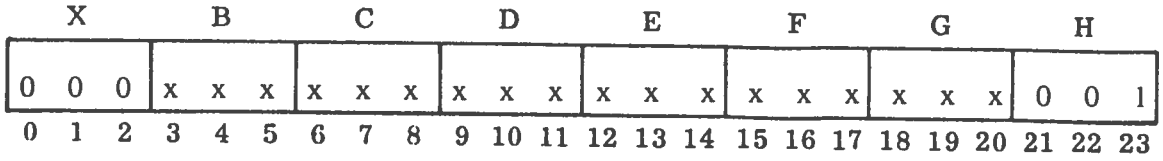
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:

ALL ZEROS

NOTES:

Zeros are loaded into the display data register and transferred to a destination specified by G. H must be changed before data may be loaded from any other source.



NAME: *SOURCE – 840A*

TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

NONE

NOTES:

Setting the octal digit H to 1 causes the display to connect its input data register input lines to the 840A interface. It will accept data from the 840A CPU only until H is changed.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *SOURCE XMEM*

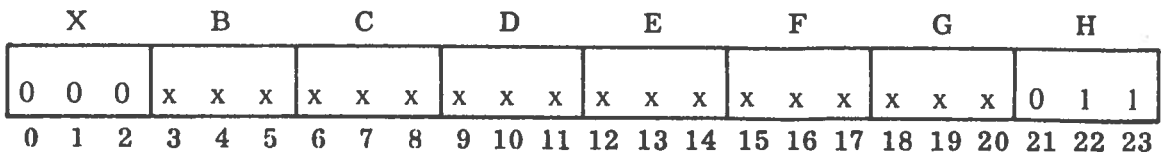
TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

NONE

NOTES:

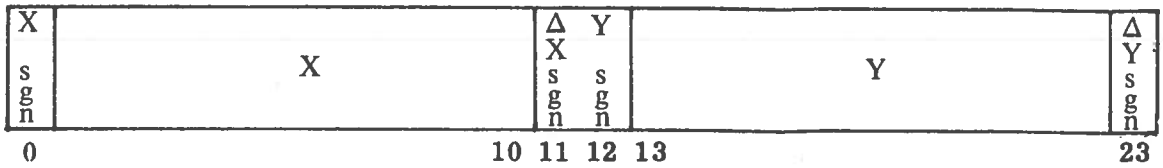
Succeeding data words transferred into the display input data register will originate from the external buffer memory until H is changed.



NAME: *TRANSFER X,Y*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

Execution of this command will cause the transfer of the contents of the X and Y registers to the display input register. The display register inputs will remain connected to X, Y and associated sign registers until H is changed. As part of the same command, the contents of X and Y will be transferred from the display data register to destination registers specified by G.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	0	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *TRANSFER EVENT COUNTER*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:

	COUNT

NOTES:

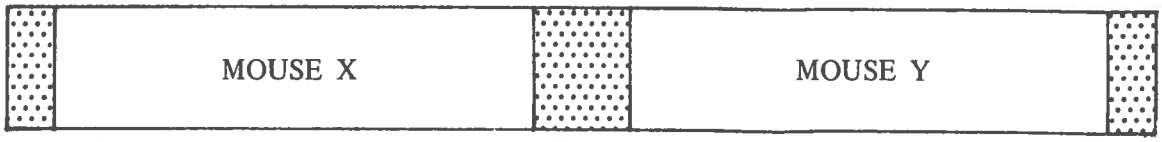
Execution of this command causes the contents of the event counter to be transferred to the display input data register and on to destination registers specified by G. The data register inputs will remain connected to the event counter until H is changed.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *TRANSFER MOUSE*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

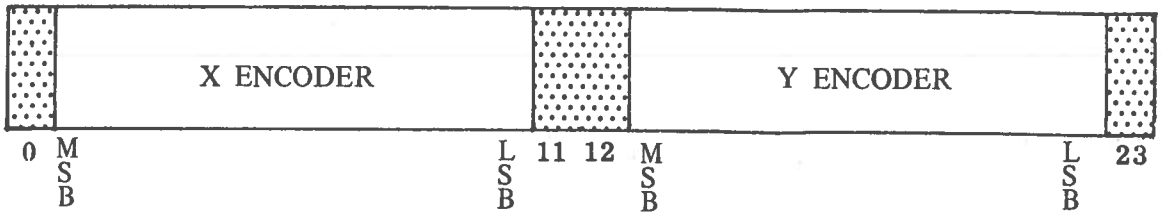
This command transfers MOUSE coordinates to display input data register and on to a register specified by G. The mouse position counters remain connected to the display data register inputs until H is changed.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *TRANSFER SHAFT POSITION ENCODERS*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

This command transfers X and Y shaft position encoders to display input register and on to a destination specified by G. Inputs of the data register remain connected to the shaft position encoders until H is changed.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *TRANSFER CONTROL SWITCHES*

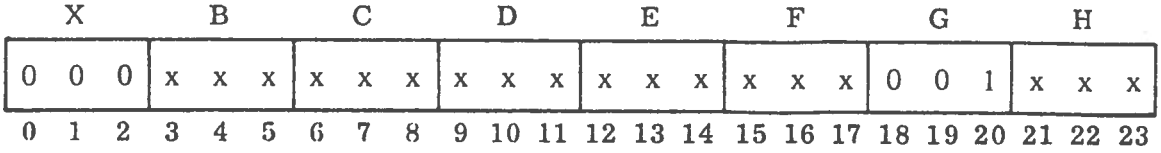
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:

24 DISPLAY CONTROL SWITCHES

NOTES:

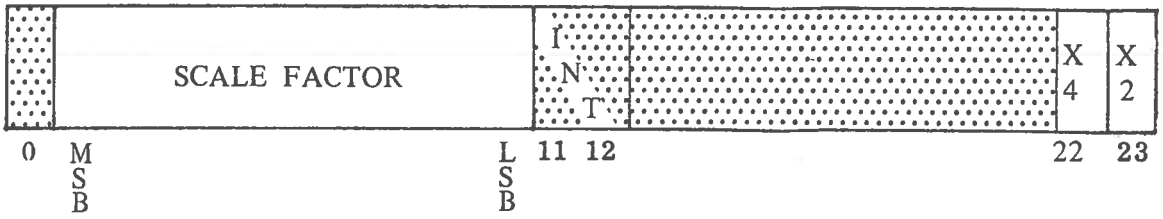
The command transfers the contents of the display control switches to the input register and on to a destination specified by G. The switches will remain connected until H is changed.



NAME: *LOAD SCALE FACTOR REGISTER*

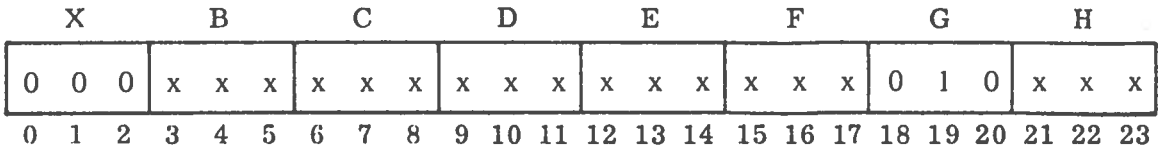
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

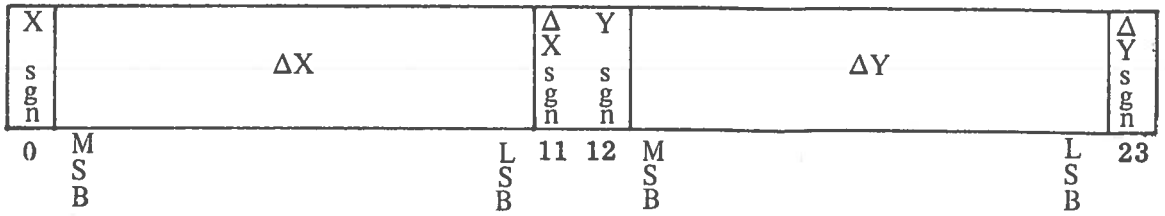
The contents of a source specified by H are loaded into the display data register and 12 bits as shown in the data format above are transferred to the scale factor register. Two bits (11, 12) are loaded into the intensity register.



NAME: *LOAD RATE REGISTERS (ΔX, ΔY)*

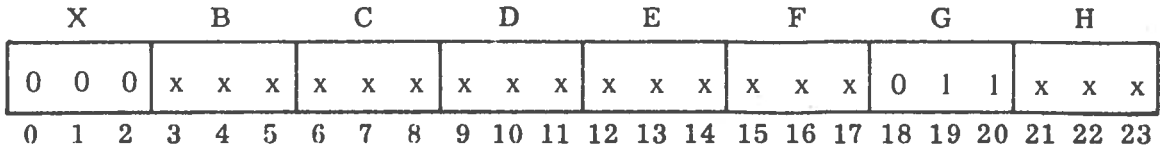
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

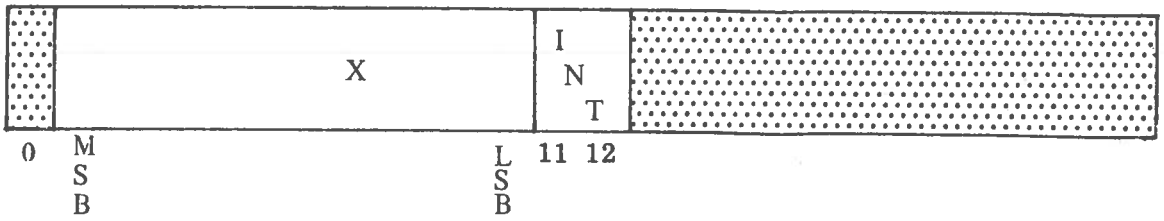
The contents of the source specified by H are transferred to the display data register and on to the rate counter ΔX, ΔY and sign registers according to the format shown above.



NAME: *LOAD X REGISTER*

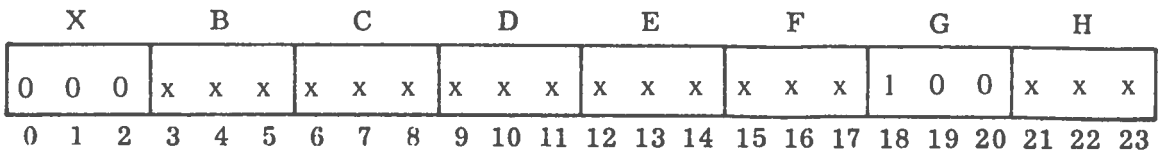
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

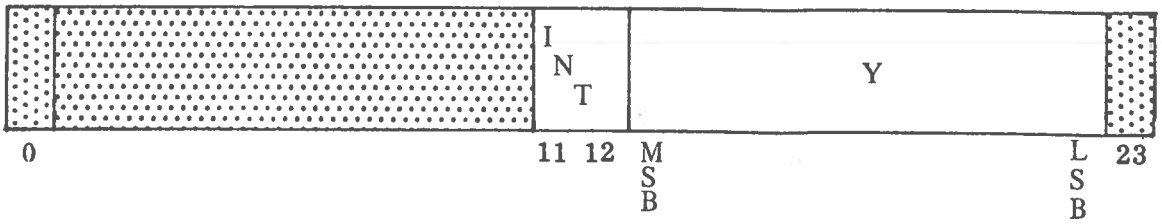
The contents of the source specified by H are transferred to the display input register and on into the X position and intensity registers according to the format shown above. All sign bits are cleared.



NAME: *LOAD Y REGISTER*

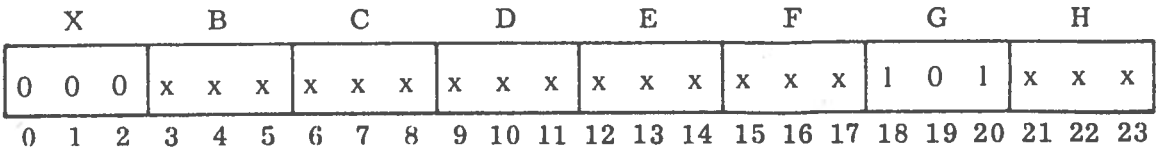
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

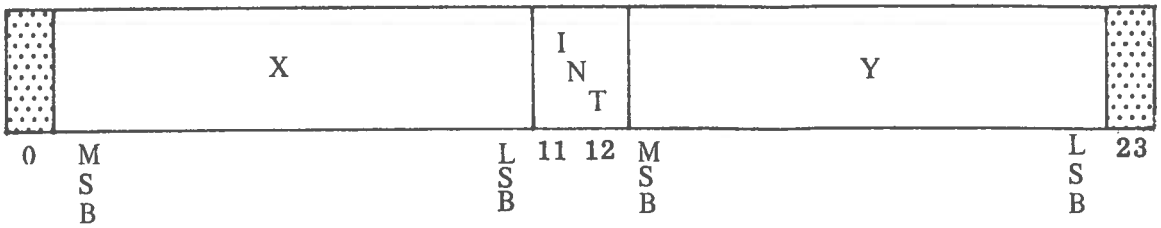
The contents of the source specified by H are transferred to the display data register and loaded into the Y and intensity registers as shown above. All sign bits are cleared.



NAME: *LOAD POSITION (X and Y) REGISTERS*

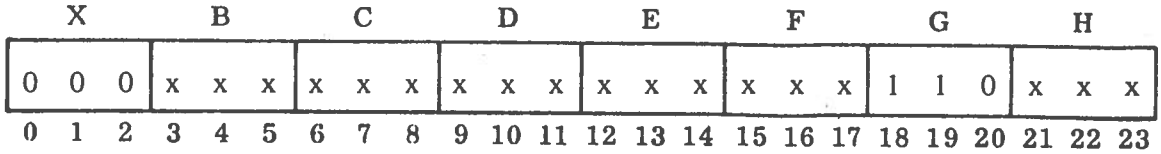
TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

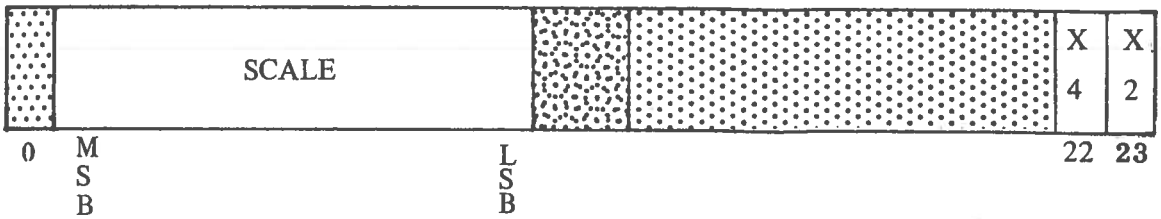
The 24-bit word specified by source digit H is transferred to the display data register and loaded into X, Y and intensity registers as shown above. All sign bits are cleared.



NAME: *TRANSFER SCALE FACTOR AND LOAD RATE REGISTERS*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

The contents of the scale factor register are loaded into the rate multiplier main counter to control the length of a line segment specified by D, E and F. The rate registers (ΔX and ΔY and signs) are loaded with a value obtained from a source specified by H.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *LOAD D/A's*

TIMING: ≈ 3 microseconds

ASSOCIATED DATA FORMAT:

D/A #1			D/A #2		
M S B		L S B	M S B		L S B

NOTES:

The contents of a source specified by H are transferred to the D register and loaded into the two non-display 12-bit digital to analog converters as shown in the format above.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *CLEAR MOUSE*

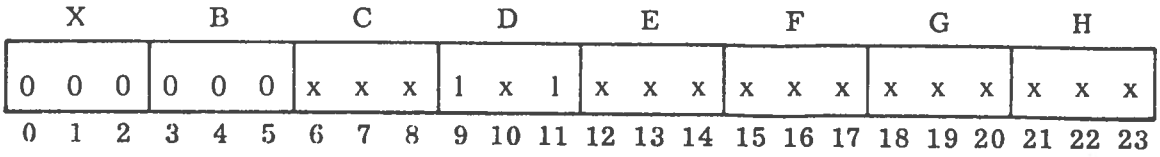
TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

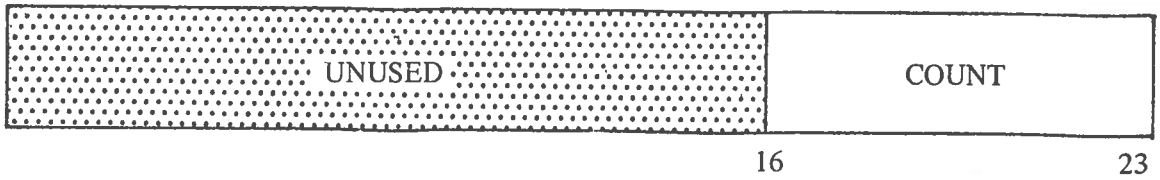
This command clears the counters associated with the MOUSE incremental encoder input device, and therefore effectively sets mouse position to the lower left corner of the display area.



NAME: *LOAD EVENT COUNTER*

TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

The event counter will be loaded on the next transfer with the number COUNT (bits 16 to 23) of the data word. The counter will count down from this value to zero and requesting an interrupt if armed.

X			B			C			D			E			F			G			H		
0	0	0	0	0	0	x	x	x	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *INCREMENT EVENT COUNTER*

TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

Note that for this command to be effective, digit B (bits 3, 4, 5) may not be set to 2 as this would clear the event counter.

DISPLAY INTERRUPTS

At the present time, two hardware priority interrupts are assigned to the display interface. These are levels 5 and 6.

Level 5, which is connected to the light pen, causes the execution of an instruction at address '105 when light is seen.

Level 6, which is connected to the display C register, causes the execution of an instruction at '106 when the display event counter reaches zero (and has been armed) or when a terminate command is loaded into the display C register.

X			B			C			D			E			F			G			H		
0	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *ARM EVENT COUNTER INTERRUPT*

TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command enables the event counter to request an interrupt on reaching a count of zero.

X			B			C			D			E			F			G			H		
0	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *CLEAR DISPLAY EVENT COUNTER AND DISARM EVENT COUNTER INTERRUPT*

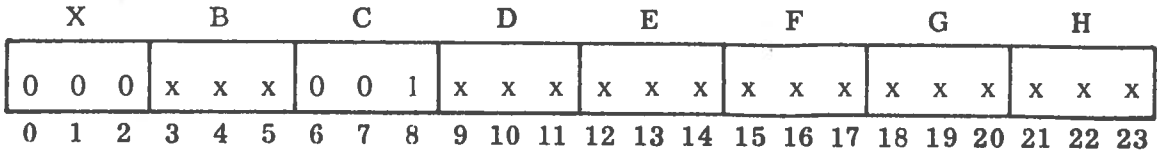
TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command is used to clear the event counter in the display. If it is desired to use the event counter as a down counter which raises an interrupt on reaching zero, an interrupt ARM command must be executed.



NAME: *START EXTERNAL BUFFER TO DISPLAY*

TIMING: ≈ 12 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command is normally only executed from the 840A CPU and is used to transfer control to external memory.

X			B			C			D			E			F			G			H		
0	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *STOP BUFFER CORE AND RAISE INTERRUPT (terminate)*

TIMING: ≈ 2 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command is used to terminate operation from external buffer core; it is not normally executed direct from the 840A CPU.

X			B			C			D			E			F			G			H		
0	0	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *STOP BUFFER CORE ON LIGHT PEN*

TIMING: N/A

ASSOCIATED DATA FORMAT:

NONE

NOTES:

If a command is issued in which digit B is 4, then any succeeding interrupt generated by the light pen will terminate operation from external buffer core. This command can be cancelled by issuing any command in which B $\neq$ 4.

MEMORY COMMANDS

The following commands and combinations of them, which are performed by executing a CEU '41 instruction, allow the 840A CPU to control the operation of the external buffer memory.

X			B			C			D			E			F			G			H		
1	x	1	x	0	x	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *INITIATE BTC TRANSFER BETWEEN 840A CORE AND EXTERNAL BUFFER CORE*

TIMING: Depends on block size and direction as well as maximum transfer rate bit.

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

If Bit 1 is present, starting address is given by bits 12–23

If Bit 3 is present, maximum rate transfer is used

If Bit 5 is a 1, transfer is XMEM to 840A

If Bit 5 is a 0, transfer is 840A to XMEM

X			B			C			D			E			F			G			H		
0	1	1	0	0	0	x	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *SET MEMORY ADDRESS REGISTER FROM 840A*

TIMING: ≈ 10 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command sets both the read and write address registers in the buffer memory to the address specified by bits 12 to 23.

If bit 6 is a 1, the memory is set to the half-cycle mode; i.e., read-clear, or write without clear.

If bit 6 is a 0, the memory is set to full cycle-mode; i.e. clear-write and read-restore.

X			B			C			D			E			F			G			H		
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *CLEAR MEMORY FROM 840A*

TIMING: ≈ 6 milliseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command initiates a buffer memory clear operation which sets all bits of all words to zero.

X			B			C			D			E			F			G			H		
0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *CLEAR ADDRESS REGISTER FROM 840A*

TIMING: ≈ 10 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

External buffer address registers are set to zero.

STORED MEMORY COMMANDS

The following two commands can be stored in external buffer memory by executing CEU '41 instructions and will actually be executed themselves only when requested by the display. These stored commands control the path of the display program through buffer core as it is being executed.

X	B	C	D	E	F	G	H
0 1 0	0 0 0	0 0 0	0 0 0	x x x	x x x	x x x	x x x
0 1 2	3 4 5	6 7 8	9 10 11	12 13 14	15 16 17	18 19 20	21 22 23

NAME: *BRANCH*

TIMING: ≈ 1.75 microseconds

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

This command, stored in external buffer memory, causes it to change its address register to the value specified in bits 12–23. It can be used to link subprograms, or to restart display loops.

X			B			C			D			E			F			G			H		
0	1	0	0	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *STORED BRANCH WITH RETURN*

TIMING: ≈ 4 microseconds

ASSOCIATED DATA FORMAT:

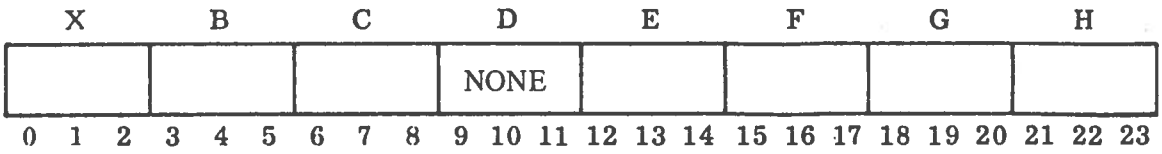
N O N E

NOTES:

This instruction, stored in external buffer, causes a branch to the address following that specified by bits 12 through 23. The address of the next sequential location in memory is stored as a return branch at the subroutine entry point.

READ-WRITE INSTRUCTIONS

This set of 840A instructions can be used for program controlled data transfer between the 840A core and the display interface. Block transfer of data is included under memory commands.



NAME: *READ XMEM TO 840A*

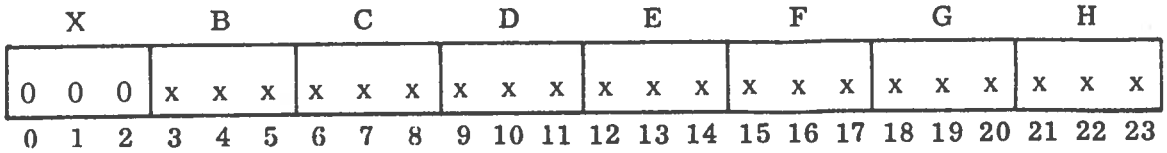
TIMING: ≈ 7 microseconds

ASSOCIATED DATA FORMAT:

24-BIT DATA WORD

NOTES:

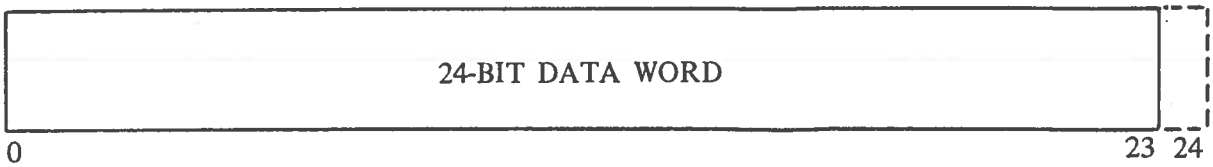
A READ will result from either an AIP '41 or an MIP '41 instruction. In either case, bit 24 of the XMEM data word will be ignored.



NAME: *WRITE 840 TO XMEM*

TIMING: ≈ 9 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

A WRITE will result from either a MOP '41 or an AOP '41, in which case bit 24 in the buffer word will be set to zero.

A WRITE will also result from the execution of a CEU '41 with bits 0–2 of word 2 set to zero. In this case, bit 24 of the stored data word will be set to 1.

X			B			C			D			E			F			G			H		
0	x	1	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *READ MODIFY WRITE FROM 840A*

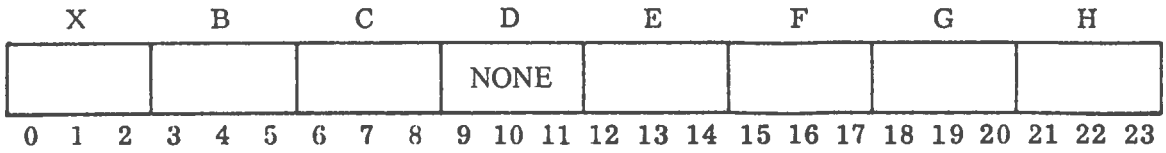
TIMING: ≈ 9 microseconds

ASSOCIATED DATA FORMAT:

NOTES:

This instruction results in a data transfer between 840A and external buffer memory. Only the zones selected are changed in external memory.

Bit 11 selects zone 1
Bit 10 selects zone 2
Bit 9 selects zone 3
Bit 8 selects zone 4



NAME: *READ FROM DISPLAY*

TIMING: ≈ 7 microseconds

ASSOCIATED DATA FORMAT:

24-BIT DATA WORD

NOTES:

Execution of an MIP '41 or AIP '40 instruction will cause a transfer of the display D register contents to the 840A CPU. Command register contents have no effect.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	1
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *WRITE TO DISPLAY*

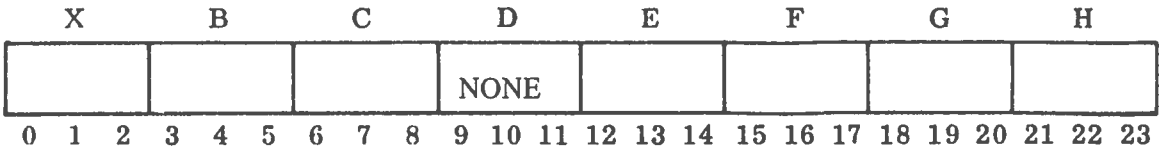
TIMING: ≈ 9 microseconds

ASSOCIATED DATA FORMAT:

24-BIT DATA WORD

NOTES:

Execution of an MOP '40 or AOP '40 instruction with the contents of the command register as shown will result in the transfer of one data word from the 840A CPU to the display D register and on to destinations determined by G.



NAME: *READ DISPLAY STATUS, KEYBOARD, BUFFER MEMORY ADDRESS*

TIMING: ≈ 5.4 microseconds

ASSOCIATED DATA FORMAT:

XMEM ADDRESS	STATUS	KEYBOARD

NOTES:

Execution of an AIP '43 or MIP '43 instruction will cause the Display Status, Keyboard and Buffer Core Address register contents to be transferred to the 840A in the format shown above.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	1	x	x	x	x	x	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *BLANK*

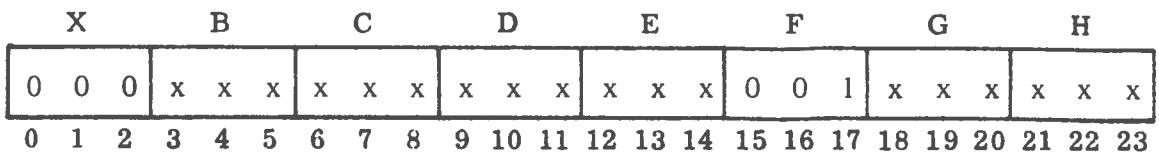
TIMING: Depends on display function being executed

ASSOCIATED DATA FORMAT:

N O N E

NOTES:

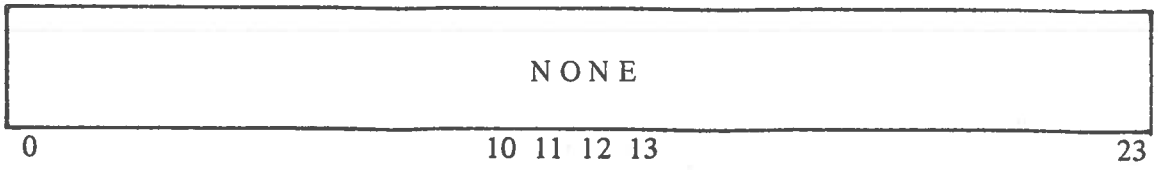
A bit in position 12 will always cause the current display function to be blanked; i.e., at zero intensity. This will continue until bit 12 is reset to 0. This same bit can be used as a pen control command for the calcomp plotter. A 1 in bit 12 means pen UP; a 0 means pen DOWN.



NAME: *LINE FEED*

TIMING: ≈ 8 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

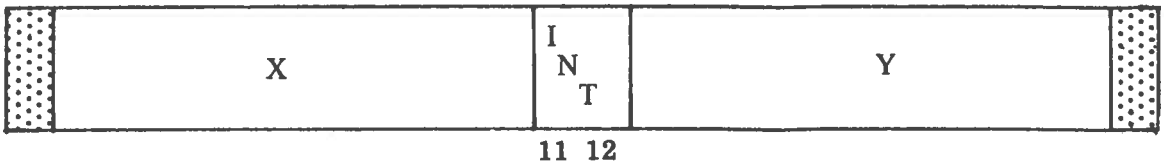
The Y register is decremented by a value equal to $\frac{1}{8}$ of full scale.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	0	1	0	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *PLOT A POINT*

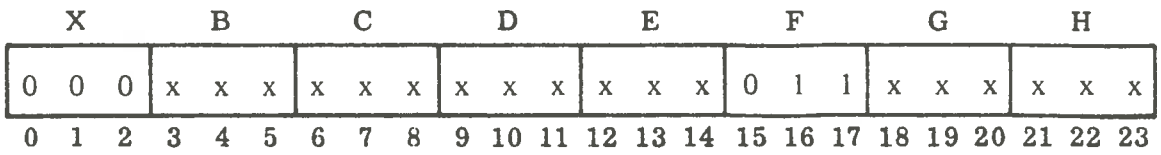
TIMING: ≈ 50 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

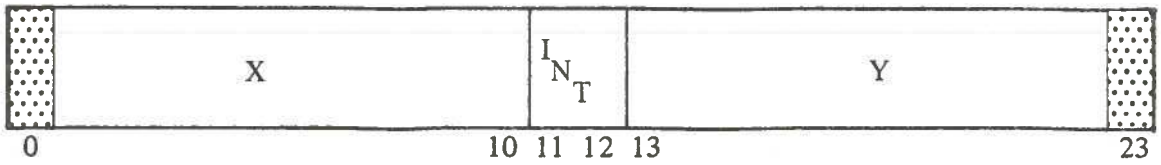
Data are transferred from a source specified by H to a destination specified by G and the contents of the X, Y and intensity registers are used to plot a point.



NAME: *PLOT ADJACENT POINTS*

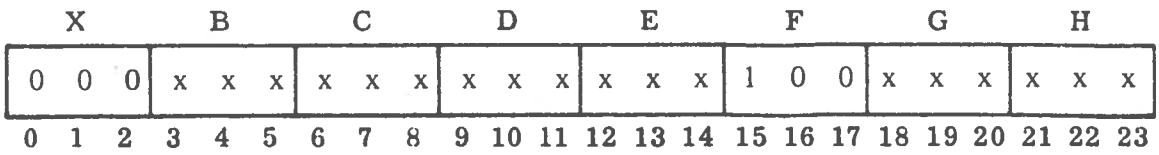
TIMING: ≈ 15 μsec/point

ASSOCIATED DATA FORMAT:



NOTES:

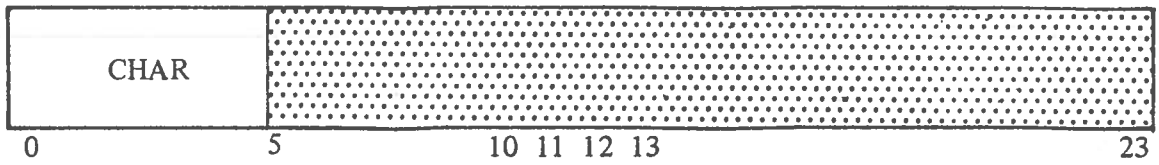
Data are transferred from a source specified by H to a destination specified by G, and the contents of the X,Y and intensity registers are used to plot a point. The point plotting time is approximately 15 μsec, so points must be closer together than approximately 1 inch.



NAME: *PLOT SINGLE CHARACTER*

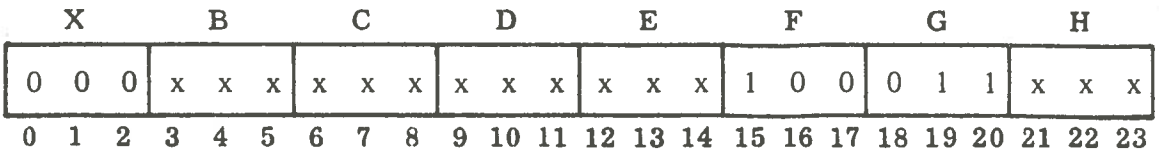
TIMING: ≈ 80 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

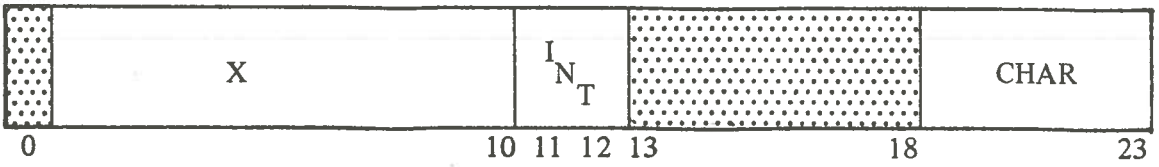
Data from a source specified by H are transferred to a destination specified by G, and the first 6 bits are plotted as an ASCII character at a position and intensity specified by X, Y, and intensity registers. If G is a 3, then the last six bits (18–23) are interpreted as a character.



NAME: *PLOT CHARACTER AND X*

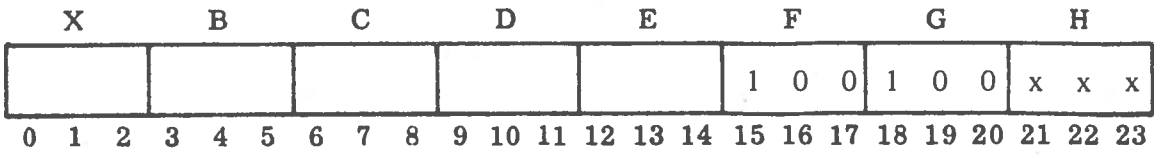
TIMING: ≈ 80 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

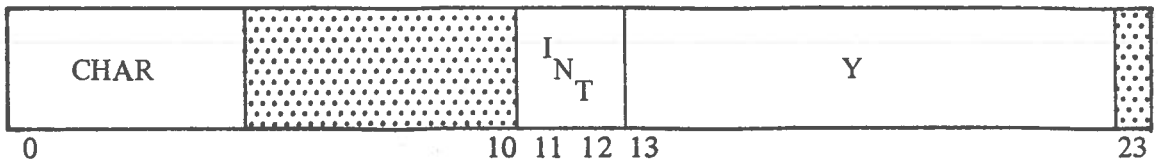
A data word obtained from source H is interpreted according to the data format shown. The display plots an ASCII character at position X and intensity as specified in the data word, and the ordinate is defined by the value in the Y register which remains unchanged.



NAME: *PLOT CHARACTER AND Y*

TIMING: ≈ 80 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

A data word obtained from source H is interpreted according to the data format shown. The abscissa is defined by the previous contents of the X register which remains unchanged.

The command will not function properly if the sign bit in the Y register has previously been left on.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	0	1	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *LOAD COLOR REGISTER*

TIMING: ≈ 10 microseconds

ASSOCIATED DATA FORMAT:

R	B	G		RED	BLUE	GREEN
0	1	2		10 11	12 13	23

NOTES:

A data word from a source specified by H is transferred to a register specified by G as well as to a 24-bit color register. The contents of the color register are interpreted according to the format shown.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1	x	x	x	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *PLOT 4 CHARACTERS*

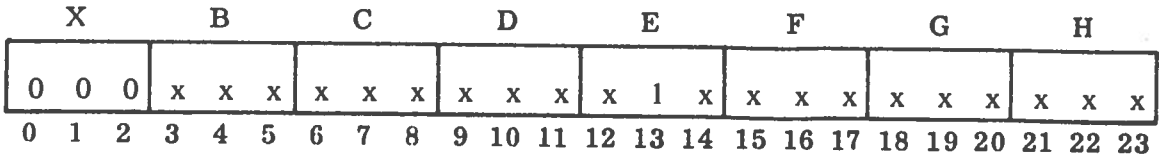
TIMING: ≈ 320 microseconds per word

ASSOCIATED DATA FORMAT:

1st CHAR	2nd CHAR	3rd CHAR	4th CHAR
0	10 11	12 13	23

NOTES:

Data words from a source H will be transferred to a destination specified by G (usually 0). The data words will also be split up into four 6-bit bytes and plotted as ASCII characters. Positioning is automatic in that X is incremented 1/64 line per character, and Y is decremented 1/8 page at the end of each line.



NAME: *HIGH SPEED PLOT*

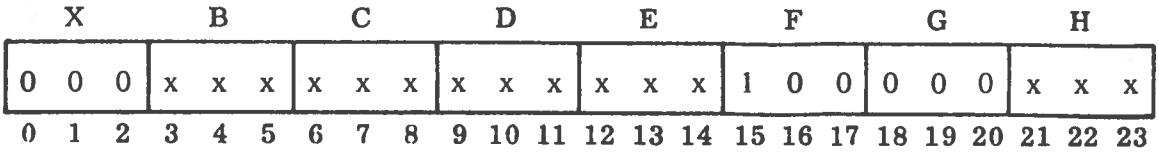
TIMING: Approx. 15 μsec/point

ASSOCIATED DATA FORMAT:

NONE

NOTES:

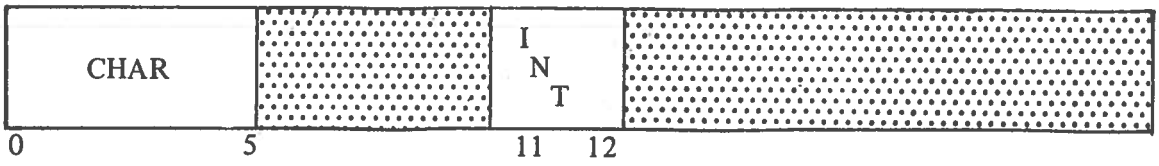
A bit in position 13 will reduce the point plotting delay from approx. 60 μsec/point to approx. 15 μsec per point. The plotting rate will remain fast until a command word is issued in which bit 13 is zero.



NAME: *PLOT SINGLE CHARACTER*

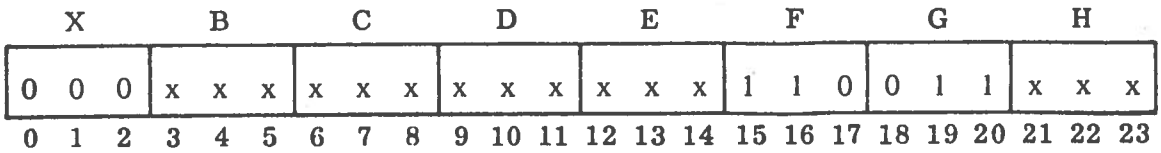
TIMING: ≈ 80 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

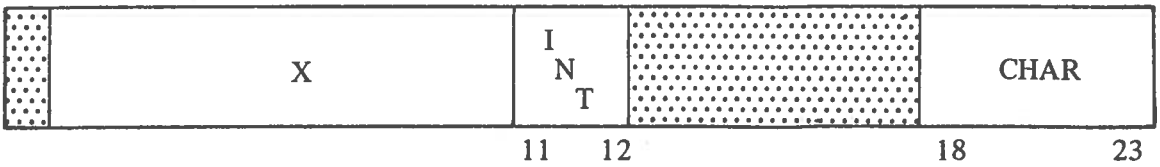
The first 6 bits (bits 0–5) of a data word from a source specified by H are used to define an ASCII character which is plotted at a position and intensity specified by the X, Y and intensity registers.



NAME: *PLOT CHARACTER AND X*

TIMING: ≈ 80 microseconds

ASSOCIATED DATA FORMAT:



NOTES:

A data word obtained from source H is interpreted according to the data format shown. The display plots an ASCII character at position X and intensity as specified in the data word, and the ordinate is defined by the value in the Y register which remains unchanged.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	1	x	1	0	0	0	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *PLOT 4 CHARACTERS*

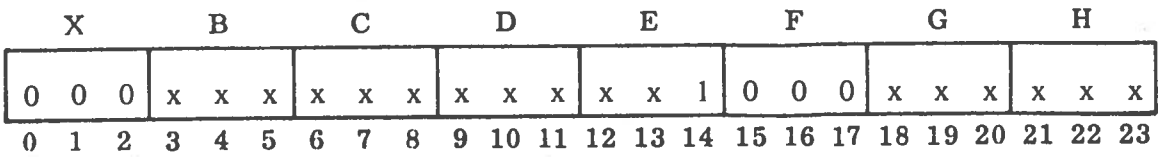
TIMING: ≈ 320 microseconds per word

ASSOCIATED DATA FORMAT:

lst Char.	2nd Char.	3rd Char.	4th Char.

NOTES:

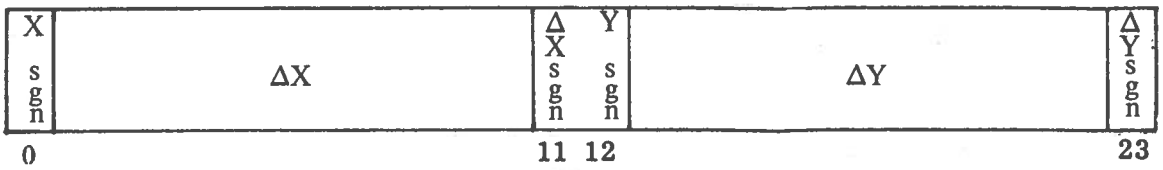
Data words from source H will be split into 4 6-bit bytes and plotted as ASCII characters. Positioning is automatic in that X is incremented 1/64 line per character and Y is decremented 1/8 page at the end of each line.



NAME: *PLOT A LINE SEGMENT*

TIMING: ≈ 10 to 4000 microseconds, depending on scale factor

ASSOCIATED DATA FORMAT:



NOTES:

A line segment is plotted from the values in the rate registers according to the format shown above. The shape of the line segment is controlled by digit D, and the values in ΔX and ΔY may be modified by the selection of source H and destination G.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	1	0	0	0	0	1	0	0	0	0	1	0	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *CIRCULAR ARC*

TIMING: ≈ 1000 microseconds

ASSOCIATED DATA FORMAT:

X sgn	ΔX	ΔX sgn	ΔY sgn	ΔY	ΔY sgn
0		10	11 12	13	23

NOTES:

A circular arc of 0 to 90° beginning at position specified by X, Y registers and with initial slope and radius determined by ΔX, ΔY and sign registers will be plotted. ΔX sign and ΔY sign should be opposite. For ΔY = zero, ΔX specifies radius.

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	0	0	1	0	0	1	0	0	0	0	1	0	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *Y PARABOLA*

TIMING: From 10 to 4000 microseconds

ASSOCIATED DATA FORMAT:

	ΔX		ΔY	

NOTES:

A parabola beginning with initial slopes determined by ΔX and ΔY and position determined by X and Y registers. The length will be determined by the scale factor register contents. The equation of the curve will be of the general form:

$$Y = K_1 + K_2(X + K_3)^2$$

X			B			C			D			E			F			G			H		
0	0	0	x	x	x	x	x	x	0	1	0	0	0	1	0	0	0	0	1	0	x	x	x
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *X PARABOLA*

TIMING: 10 to 4000 microseconds

ASSOCIATED DATA FORMAT:

SAME AS Y PARABOLA

NOTES:

Same as Y parabola except that the equation would be:

$$X = K_1 + K_2(Y + K_3)^2$$

X			B			C			D			E			F			G			H		
0	0	0	0	1	1	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	1	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *PLOT A BLANK SCALED VECTOR FROM SHAFT POSITION ENCODERS, AND ARM AND INCREMENT EVENT COUNTER*

TIMING:

ASSOCIATED DATA FORMAT:

VECTOR FORMAT

NOTES:

In octal '3035066

X			B			C			D			E			F			G			H		
0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

NAME: *INITIATE XMEM OPERATION, PLOT 4 CHAR MODE FROM XMEM AND CLEAR EVENT COUNTER AND MOUSE*

TIMING:

ASSOCIATED DATA FORMAT:

lst Char	2nd Char	3rd Char	4th Char

NOTES:

In octal – '2160502