A solar radio polarimeter

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A SOLAR RADIO POLARIMETER

- G. R. MISNER AND L. R. McNARRY -

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ABSTRACT

A time sharing polarimeter for studies of the polarization of solar radio bursts in the meter-wavelength range is discussed. Particular attention is paid to the electronic circuitry involved.

CONTENTS

FIGURES

TABLES

A SOLAR RADIO POLARIMETER

– G.R. Misner and L.R. McNarry –

INTRODUCTION

The solar radio polarimeter to be described is used at the Algonquin Radio Observatory for studies of the polarization of solar radio bursts. This system is a redesigned version of a previous polarimeter [1]. The heart of the system is the electronic switch where the RF signals from the pair of cross-polarized antennas are combined to produce six components of polarization. These are

A	intensity from antenna A
B	intensity from antenna B
V	intensity of vertical component
H	intensity of horizontal component
R	intensity of right-hand circular component
L	intensity of left-hand circular component

The six polarization components are recorded on six channels of an eight-channel chart recorder and also on an instrumentation tape recorder. The magnetic tape is used as an input to a computer, which processes these polarization components and gives the intensity of the burst, the percentage of polarization, the degrees of linear and circular polarization, the orientation angle and axial ratio of the polarization ellipse; and also, if desired, the intensities of the unpolarized, polarized, circular, and linear components.

DESIGN MOTIVES

This polarimeter was designed to have greater accuracy than a previous polarimeter. Hybrid junction phase shifters and attenuators in the electronic switch assure a greater degree of accuracy than is obtainable with standard components. Integrated circuits and transistors are used extensively to improve the reliability. Only two tubes are used in the system and these are the noise diode tubes.

The noise diode calibration circuit is automated to reduce errors due to operator judgment and also to reduce the normal observing routine. Other functions have been automated for the same reasons.

The polarimeter is also designed so that it can be controlled from a remote location. It has been used on the 46-meter telescope at the Algonquin Radio Observatory, and was located at the prime focus of the paraboloid, while the outputs and controls were located in the control building.

GENERAL DESCRIPTION OF THE SYSTEM

A cross-polarized log-periodic antenna that has a frequency range of 50 to 500 MHz is used on a motor-driven equatorial mount that automatically follows the sun throughout the day. Provision is made to rotate the antenna through 45° about its axis to determine and assess the effect of ground reflections. Solid sheath coaxial cables are used between the antenna and the polarimeter to reduce signal attenuation and interaction between the two RF signals. The block diagram of the polarimeter is shown in Fig. 1.

The *noise diode calibration circuit* is used to calibrate the polarimeter. It produces two non-coherent RF noise signals of equal amplitude which are fed independently to the RF receivers and consequently produce output voltages on each of the data channels that should be equal. The noise diode calibration is used by the computer to compensate for differences in gain and linearity of the individual channels and thus produce identical scaling for all the data channels; the scaling units are noise diode milliamperes.

The *RF system* amplifies the input signals and converts these signals to the IF frequency, 10.7 MHz. The phase and amplitude relationships of the two RF amplifiers must be equal, and the dynamic range of the amplifiers must be wide. Various center frequencies may be used in the polarimeter by merely changing the RF amplifiers.

The *commutator* produces the switching waveforms necessary to control the electronic switch and time demodulators.

The *electronic switch* produces the polarization intensity components by combining the outputs of the two RF amplifiers, A and B, with various amplitude and phase relationships. The output of the electronic switch is a 10.7 MHz signal with the polarization intensity components V, H, R, L, A, and B occurring in this sequence at a rate of 200 times a second.

The output of the electronic switch is fed through the *automatic attenuator*, which inserts or removes attenuation in 3-db steps up to a maximum attenuation of 45 db depending on the output of the IF amplifier. This circuit is necessary because of the small dynamic range of the instrumentation tape recorder that is used with the system.

Normally, two *IF amplifiers* are used in the polarimeter. One has a bandwidth of 10 kHz and the other 20 kHz. The two bandwidths are used in Faraday rotation experiments. Each IF amplifier has a square law detector and a buffer amplifier.

In the *time demodulators*, the outputs of the square law detectors are synchronously detected relative to the electronic switch, then filtered and buffered for each channel. Filter time constants of 0.1, 0.5, and 1.0 sec may be selected by a switch.

A detailed discussion of each circuit follows.

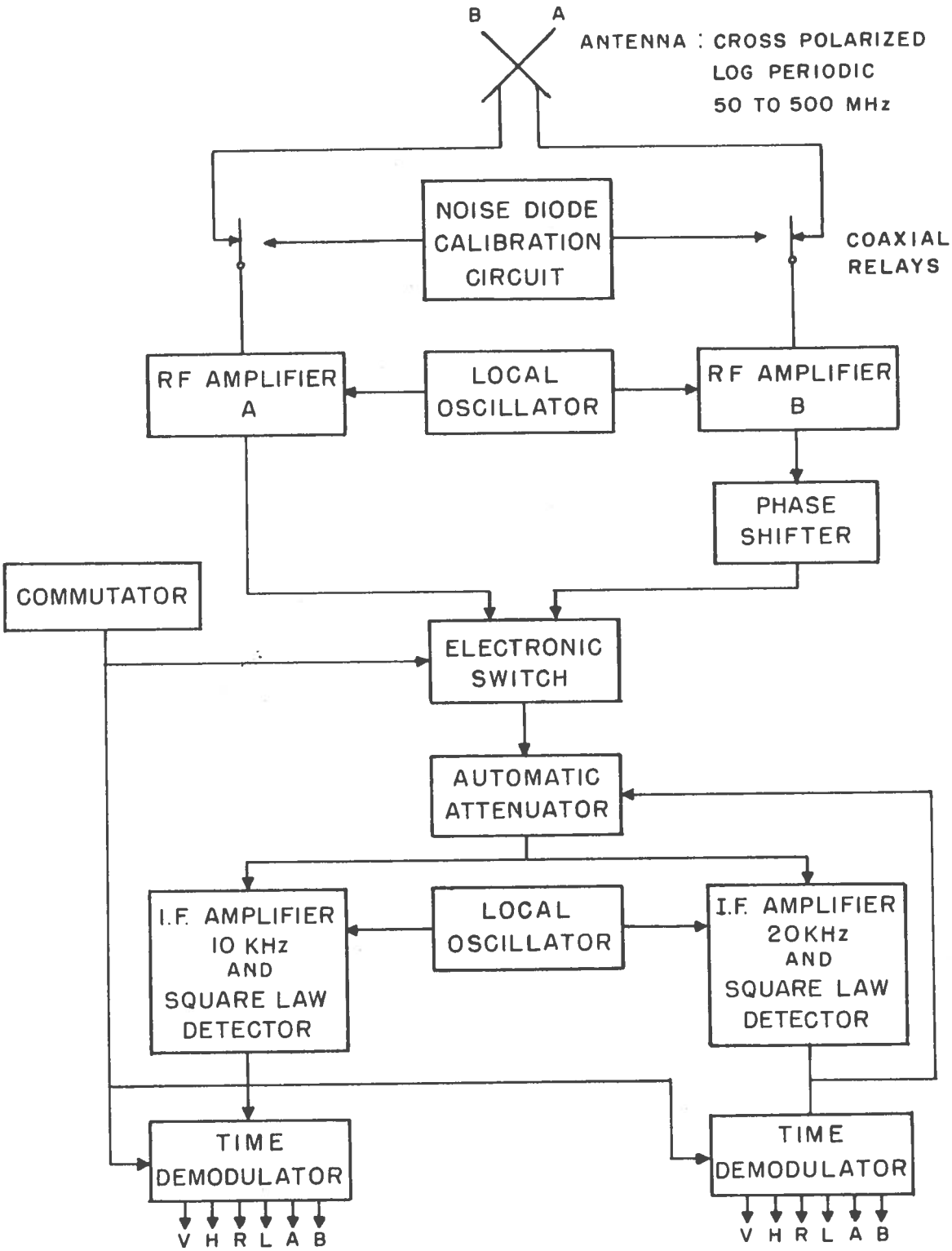


Figure 1 Polarimeter block diagram

CIRCUIT DESCRIPTIONS

The Noise Diode Calibration Circuit

A noise diode calibration of the system is done at the beginning and at the end of the observing period. The system is also calibrated on each hour to check that the gain of the polarimeter does not vary throughout the observing period.

The noise diode calibration circuit provides levels of 0, 5, 10, 15, 20, 25, 0 mA of noise diode currents. Each current level is maintained for 1 minute for the normal calibration and for 10 seconds for the hourly calibration. The current levels should produce equal voltages on each of the output data channels as shown in Fig. 2.

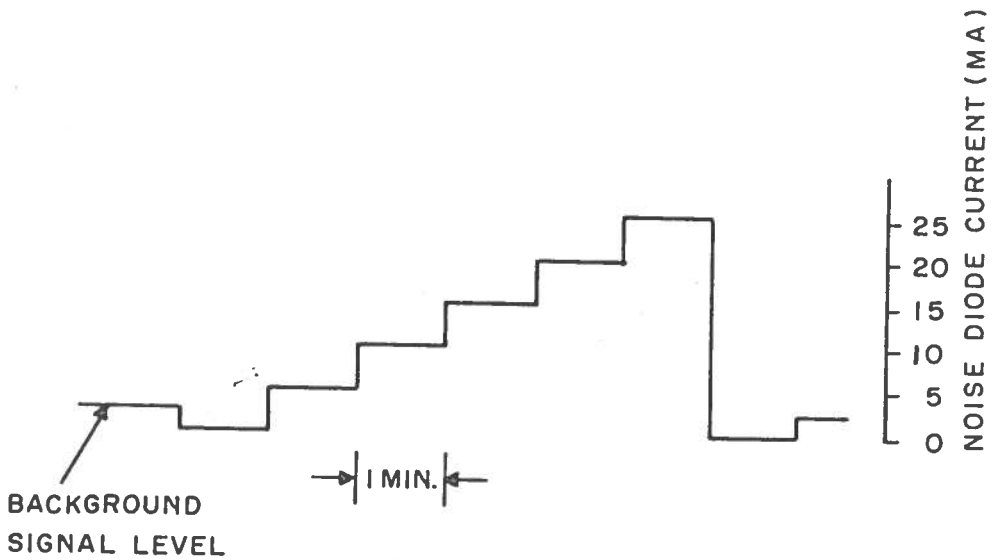


Figure 2 Output of a time demodulator channel during a noise diode calibration

The circuit regulates the filament current of a temperature limited noise diode to produce the desired plate currents. The RF noise output of the noise diode is a function of the temperature of the diode's filament and, therefore, a function of the filament current. Two noise diodes are used in order that no phase information will be contained in the calibration; that is, the noise input to the receivers must not be coherent.

This circuit has three modes of operation: manual start and stepping, manual start with automatic stepping, and remote start and stepping. The circuit turns itself off after the last zero step. The automatic and remote functions require switch closures in an external timer. The manual start and stepping is used for polarimeter testing, and the manual start with automatic stepping is used for the normal calibration. The remote start and stepping produces the calibration on the hour. A switch closure on the hour initiates the sequence, and a switch closure at 10-second intervals steps the circuit.

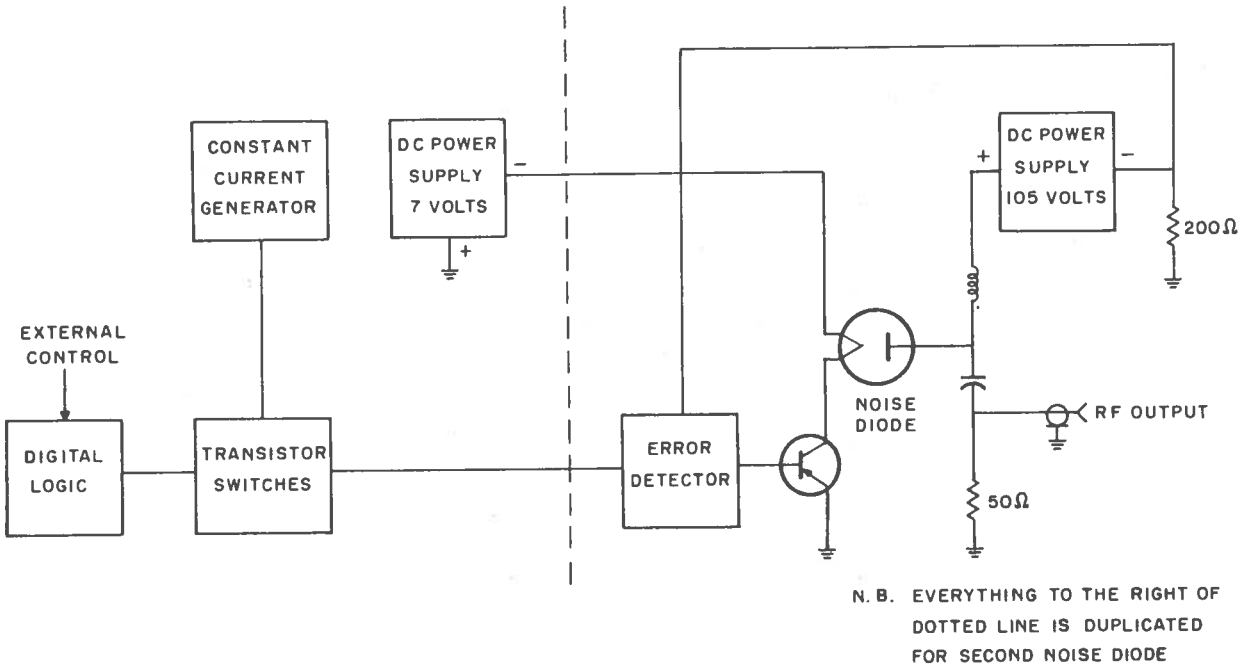


Figure 3 Noise diode calibration circuit block diagram

The block diagram, Fig. 3, shows the basic parts of the circuit and Fig. 4 is the schematic diagram. A description of each follows.

dc Power Supply +105 V

There is a separate high-voltage supply for each noise diode. These zener diode regulated supplies are floating because it is necessary to use a 200-ohm 1% resistor between ground and the negative side of the supply as the plate current sensing resistor. A meter may also be switched into the circuit to measure the plate current.

dc Power Supply -7 V

This supply is an unregulated full-wave supply that feeds the filaments of both noise diodes.

Control Circuit

The function of the control circuit is to produce a stepped voltage that is used to control the current through the noise diode. This control circuit consists of the digital logic, transistor switches, and relays K1 and K2. The digital logic circuit counts the number of switch closures at its input and turns on the transistor switches sequentially. A stepped voltage is produced by the constant current flowing into the various resistors in the collector circuits of the transistor switches. The positive supply (+3.6 V) connection is made to the logic circuit at all times but the chassis common is not. Pushing

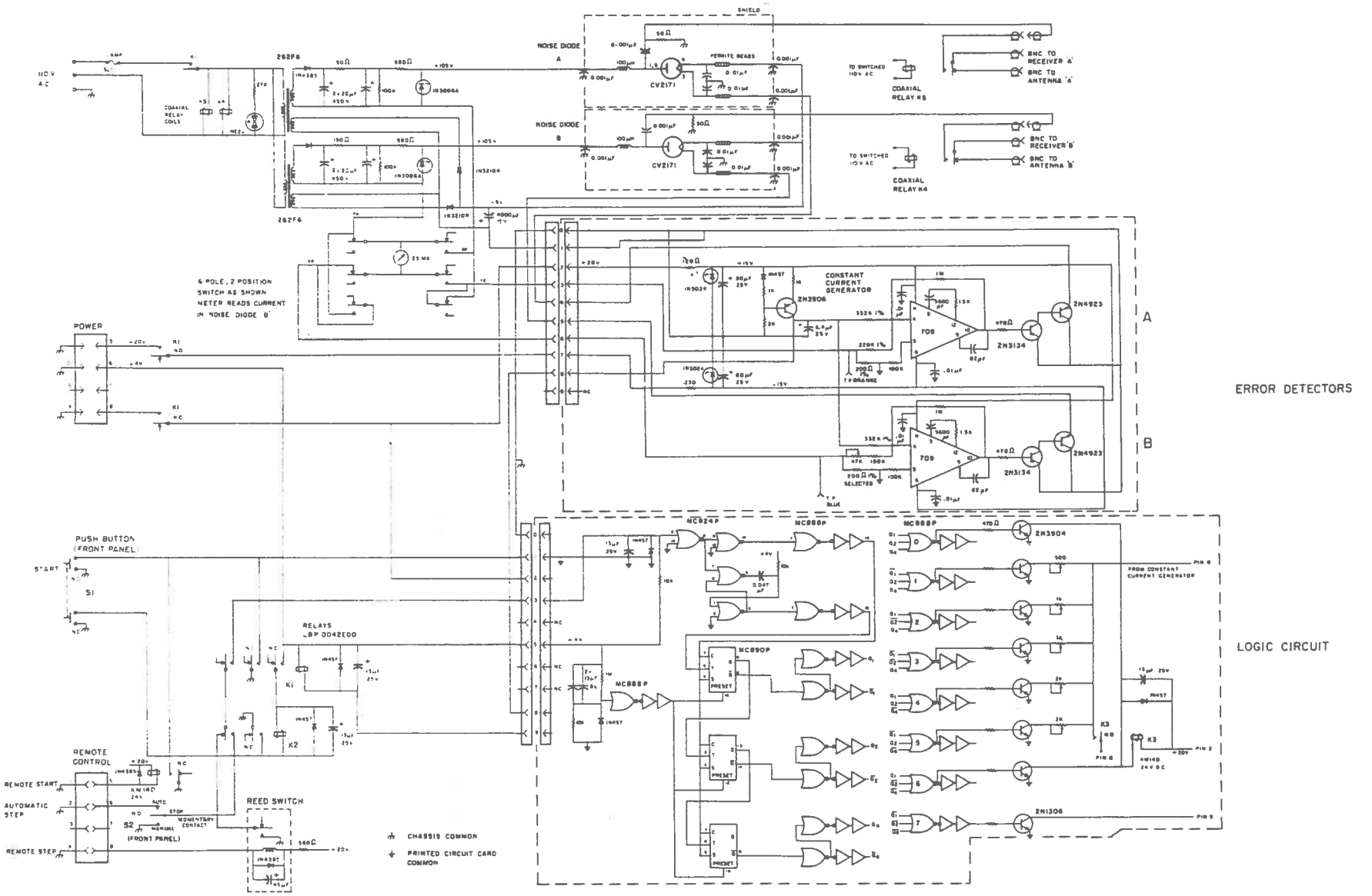


Figure 4 Schematic diagram of noise diode circuit

the start button, S1, or having the remote start contact taken to the chassis common completes the power circuit to the card. A differentiating network combined with a buffer (MC888P) produces a pulse that presets all the JK flip-flops (MC890P) to the logic 0 state (i.e., Q = 0) whenever power is applied to the circuit. The decoded output of the JK flip-flops turns on the transistor associated with gate 0 and also, because of the phase inversion in gate 7, turns on the transistor associated with gate 7. The latter transistor pulls in relay K1 which latches the logic circuit common to the chassis common, and thus power to the card is maintained.

The JK flip-flops are normally kept in an inhibit mode to reduce false switching by keeping the SET and CLEAR terminals in the logic 1 state. When the input line is shorted to the chassis common, the SET and CLEAR inputs are taken to the logic 0 state. Also, this pulse is applied to a monostable multivibrator whose output feeds the toggle input of the first JK flip-flop. The three flip-flops are connected as a simple ripple counter. Buffer elements are used to increase the fan-out capabilities of the logic elements. The count stored in the JK flip-flops is decoded by eight 3-input gates (MC888P). Gates 0 and 6 pull in relay K3 whose contacts take the output of the constant current generator to ground. Gates 1 through 5 insert resistances between the constant current generator and ground. Thus a voltage step function is developed and this signal is applied to the error detector.

When gate 7 is turned on, relay K1 drops out, cutting off the power to the logic circuit. Relay K1 also controls the power, 110 V ac, +20 V, and -20 V to the chassis.

The manual start pushbutton, S1, also activates another relay, K2, that switches the input to the logic circuit from the remote stepping contacts to the front panel stepping switch. In other words, when relay K2 is activated the logic circuit stepping is controlled by the front panel switch S2. This switch can be used to step the circuit manually or, when it is in the automatic position, external switch closures step the circuit.

The remote start and stepping contacts are also used to control the noise diode circuit from a remote location. When the polarimeter was used on the 46-meter telescope, it was necessary to use relays because of the resistance of the lines between the focus and the control building of the 46-meter telescope. A reed relay is used for the remote stepping to reduce the noise when the circuit is operated normally, as this relay is activated every ten seconds and the noise from an ordinary relay could not be tolerated.

Error Detectors

The function of the error detector is to control the filament current of the noise diode to produce the required noise diode current. There are two error detectors, one for each noise diode, and the constant current generator on the printed circuit card. (Refer to the schematic diagram of the noise diode circuit, Fig. 4.) The constant current

generator produces a current of approximately 5 mA, which is fed to the transistor switches in the logic circuit. The stepped voltage developed by the transistor switches is applied to both error detectors A and B.

The error detector controls the filament current of the noise diode to produce a diode current such that the voltage developed across the 200-ohm sensing resistor is linearly related to the voltage developed by the transistor switches. The voltage across the sensing resistor is negative while the stepped voltage from the transistor switches is positive. An integrated-circuit operational amplifier (709) adds these two voltages together to produce an error voltage. This error signal is fed into a complementary Darlington compound that supplies the necessary current gain to control the noise diode filament current.

There can be some differences between the two error detectors and noise diode tubes and these will result in different currents flowing through the two noise diodes. This is overcome by adjusting the summing resistor in error detector B to make the diode currents equal. The diode currents are controlled to better than 0.1 mA.

RF Noise Diodes

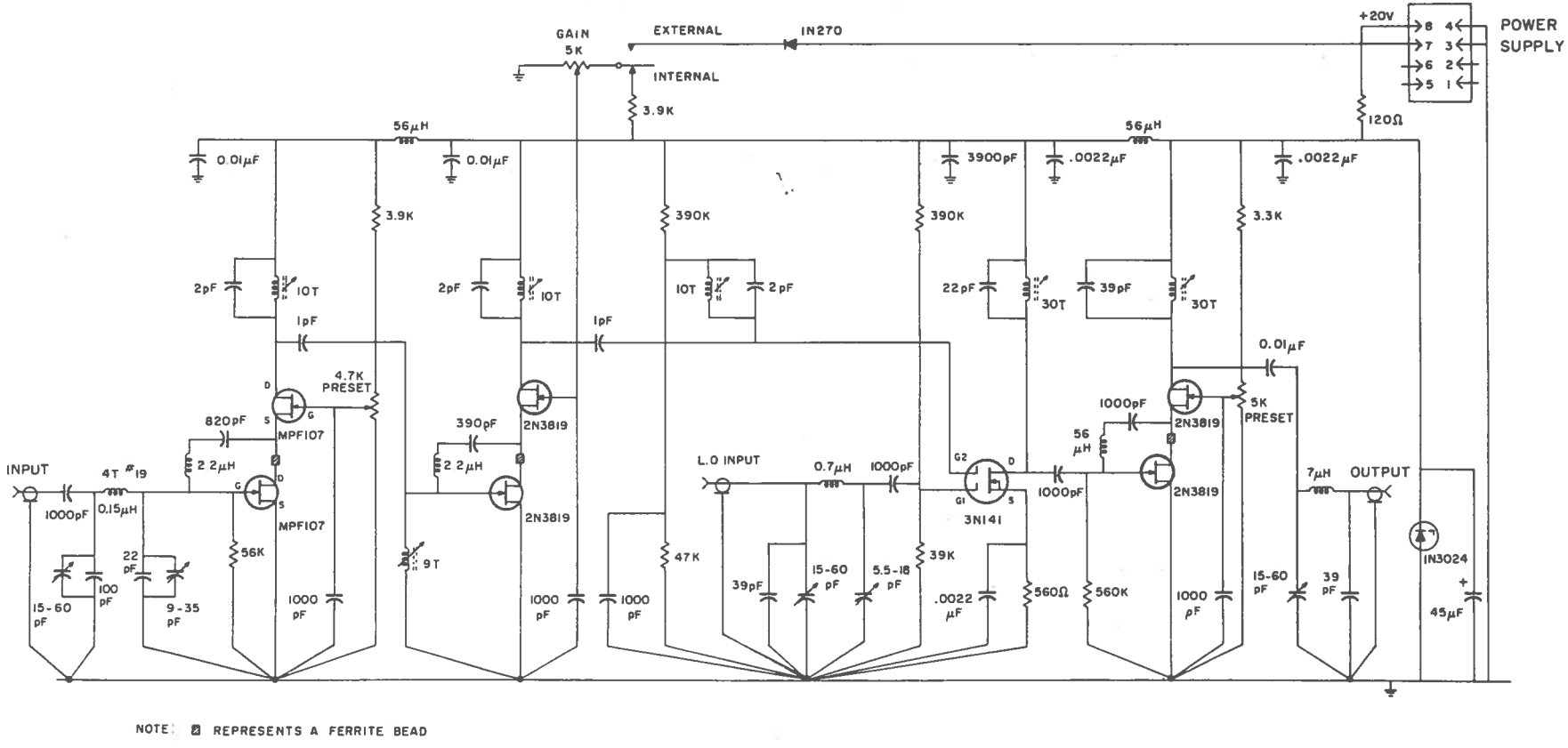
Care is taken to match the noise diode outputs to 50 ohms. The VSWR's are less than 1.02/1.00.

The RF System

The RF section of the polarimeter amplifies the signals from the antenna and converts them to the IF frequency. It consists of two RF amplifiers, a common local oscillator, and a phase shifter. It is important that the phase and amplitude relationships between the RF amplifiers be equal. The amplitudes can be adjusted by the gain controls of the RF amplifiers. A hybrid junction phase shifter in the output of one of the RF amplifiers allows the phase to be adjusted. This phase shifter is electronically controlled for remote operation of the polarimeter.

The 73.8-MHz amplifiers, that are normally used in the polarimeter, use field effect transistors (FET) in neutralized cascode circuits. The schematic diagram is shown in Fig. 5. There are two stages of RF amplification. The preset gain control of the input stage is adjusted for optimum noise figure, and it also has a small effect on the input matching. The mixer uses a dual insulated-gate FET. The resulting IF signal is amplified in a neutralized cascode stage. For remote operation of the polarimeter, the gain may be controlled externally by a dc voltage.

The common local oscillator operates at 63.1 MHz. The two outputs of the oscillator are isolated by FET cascode stages to prevent interaction between the two receivers. The isolation is of the order of 60 db.



NOTE: ▣ REPRESENTS A FERRITE BEAD

Figure 5 Schematic diagram of 73.8-MHz RF amplifier

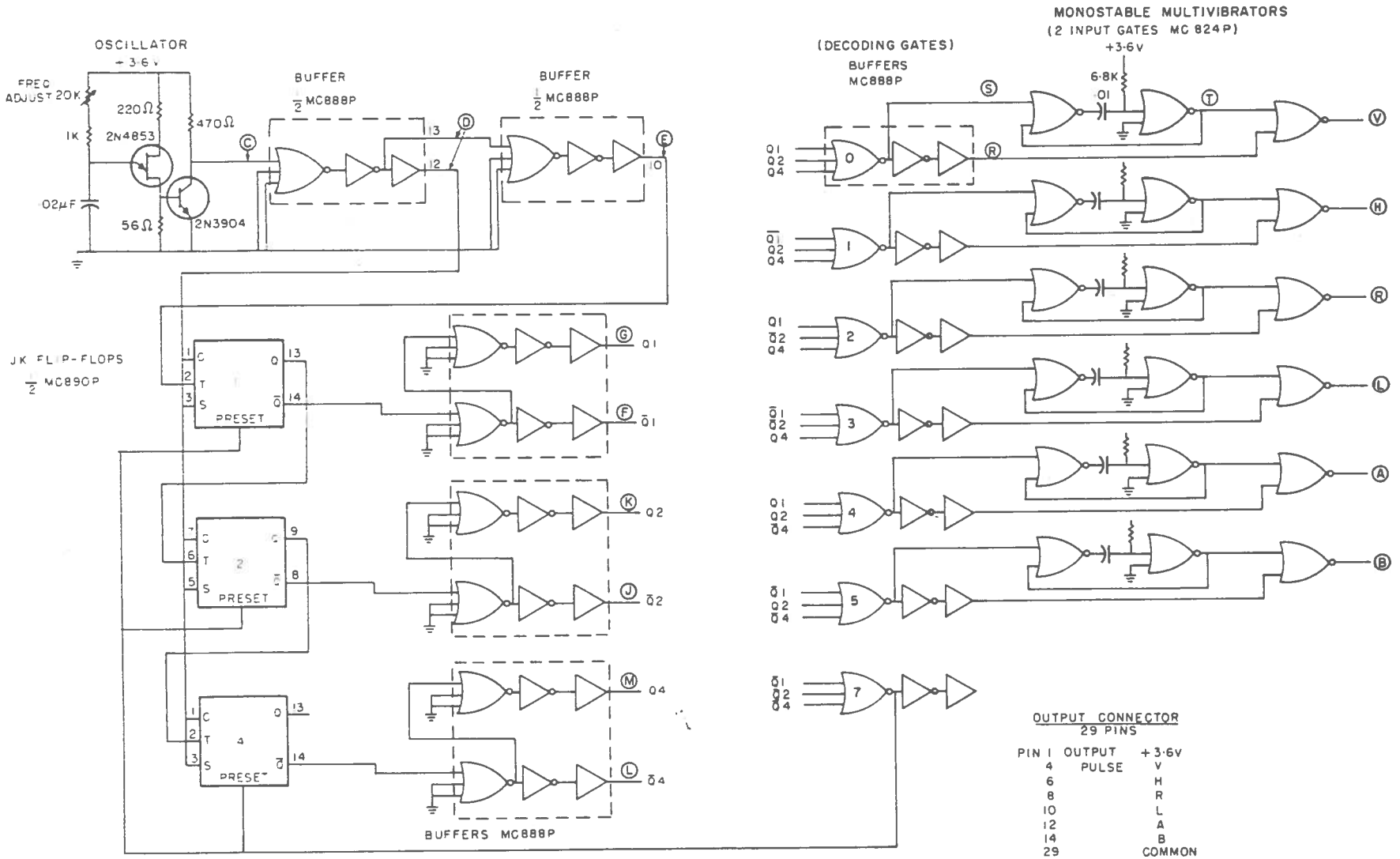


Figure 6 Schematic diagram of commutator

The specifications for the RF amplifiers are listed in Table I.

TABLE I

Specifications of RF Amplifiers

Center frequency	73.8 MHz
Bandwidth	$>$ 300 kHz
Output frequency	10.7 MHz
Noise figure	$<$ 2.8 db (T system $\approx$ 260°K)
ΔT minimum	4.2°K (for an IF bandwidth of 10 kHz)
Dynamic range	$>$ 40 db
Gain	60 db
Relative phase shift between amplifiers	$\pm 3°$ over 40 db dynamic range
Relative amplitude between amplifiers	within 3% over 40 db dynamic range
Crosstalk between amplifiers	$<$ 50 db

The Commutator

The commutator produces the pulses necessary to synchronize the electronic switch and the time demodulators. These are sequential pulses available from six output lines, called V, H, R, L, A, and B. Figure 6 is the schematic diagram of the commutator and Fig. 7 gives the waveforms to be found at the lettered points in the circuit.

Because of its simplicity, a unijunction oscillator is used to produce the timing pulses in the commutator circuit. The frequency of the oscillator is 7 times that of the commutator. The commutator frequency is normally 200 Hz but may be varied between 100 and 1000 Hz.

The logic circuit, using RTL integrated circuits, is basically a ring counter. The output of the unijunction oscillator is buffered and applied to the SET and CLEAR terminals of the JK flip-flops and also to another buffer. The flip-flops are normally held in the inhibit mode (SET and CLEAR are high) by the first buffer. The second buffer feeds the toggle input of the first flip-flop and produces a small time delay of the toggle pulse relative to the pulse that is applied to the SET and CLEAR terminals. The toggle inputs of the other flip-flops are fed from the Q output of the preceding flip-flop.

The seven gates (3-input NOR gates) decode the count in the flip-flops to the decimal system. The output of each of these gates goes to a monostable multivibrator, whose period

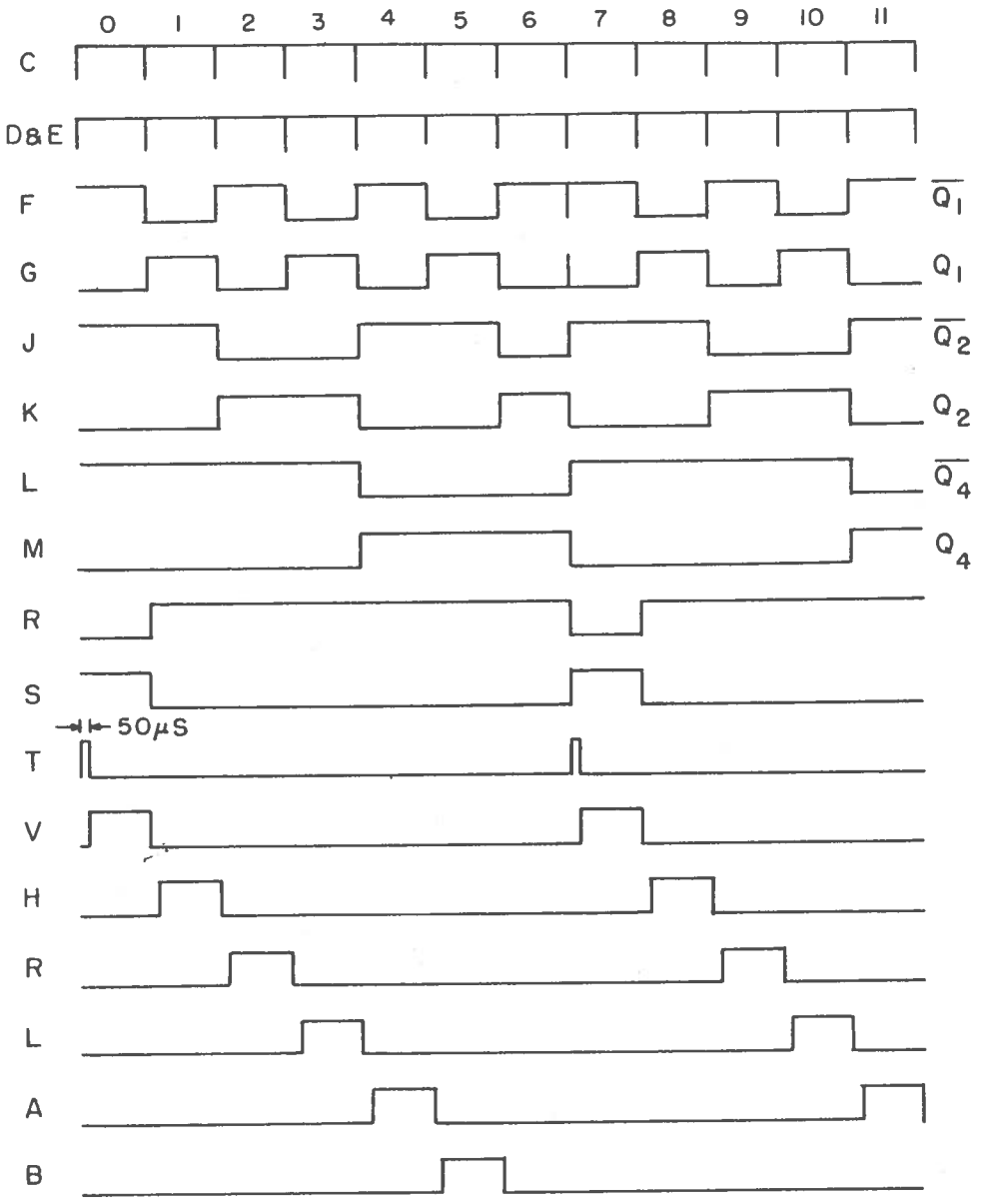


Figure 7 Commutator waveforms

is 50 μsec, and to an inverting amplifier. The outputs of both devices are applied to a 2-input gate. The output of this gate is the decoded pulse delayed by 50 μsec. This delay prevents overlapping of the channels due to the response time of the IF amplifiers. The count of six is not decoded. This allows a blank space between one set of polarization components and the next in order to make identification of the output channels easier. When the count of seven occurs, the JK flip-flops are reset to the zero state (Q's are 0) and the sequence is started over again.

The Electronic Switch

In the electronic switch, the six polarization components are produced by combining the outputs of the two RF amplifiers with the necessary phase and amplitude relationships. The block and schematic diagrams of the electronic switch are shown in Fig. 8.

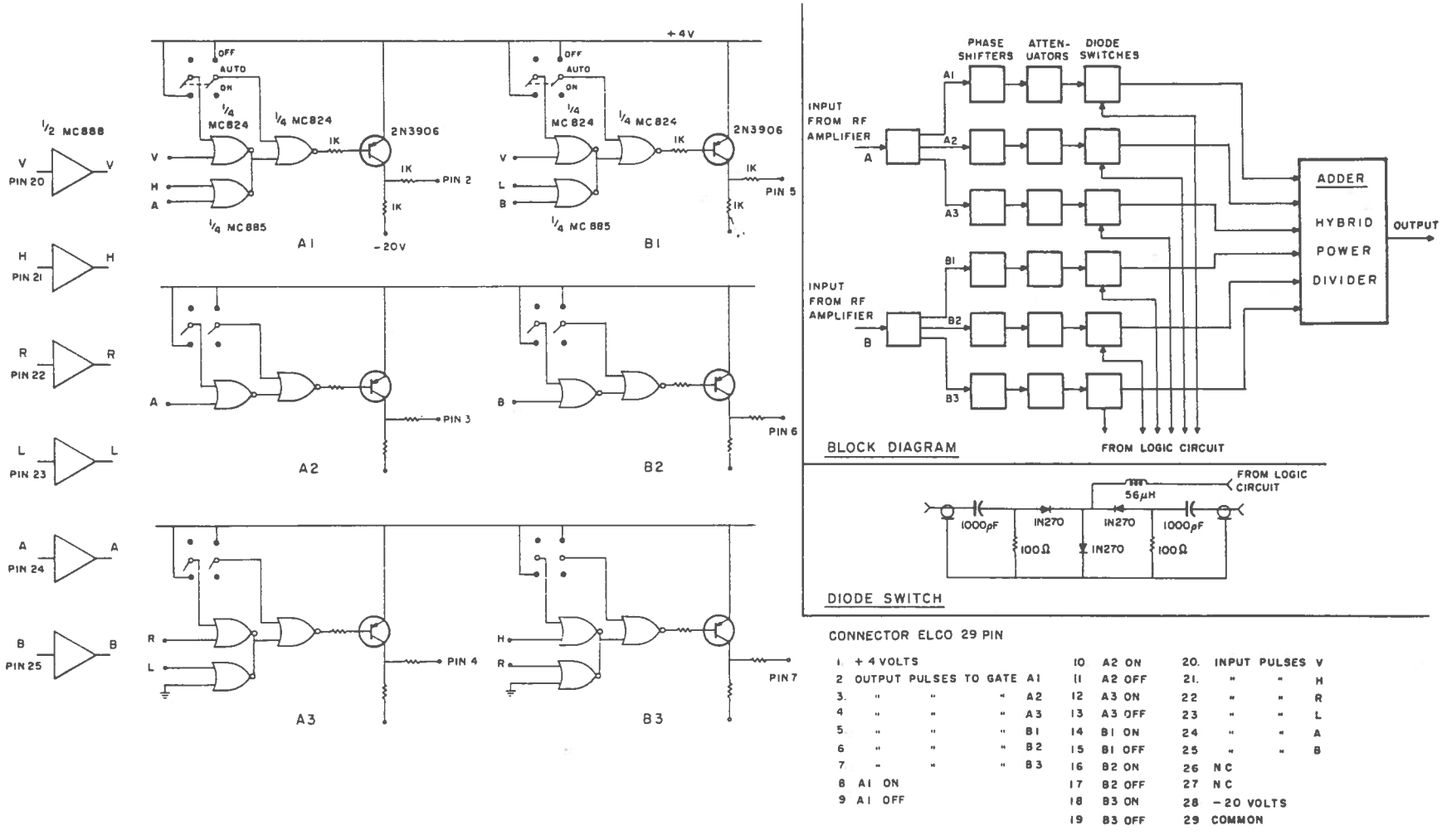


Figure 8 Schematic diagram of electronic switch

At the input to the electronic switch, the signals from RF amplifiers A and B are fed into power dividers that split each signal into three components with an amplitude balance of 0.2 db and a phase balance of 1.0°. The power dividers have a coupling loss of 6 db.

At the output of the power dividers there are six signals called A1, A2, A3, B1, B2, and B3. Each one of these signals is fed into a phase shifter, an attenuator, and a diode switch. The phase shifters are manually operated hybrid junction devices with a phase shift range of 0 to 210° with an amplitude variation of less than 1 db across this range. The attenuators have a phase variation of less than 1° from minimum to maximum (0 to 25 db) attenuation. The phase and amplitude adjustments are, therefore, almost independent of one another.

The diode switch turns the desired channels on or off. The isolation of the switch is greater than 50 db. A positive voltage on the control line turns the switch off and a negative voltage turns the switch on. A logic circuit determines when the switch should be on or off. The switching sequence to produce the desired polarization components is shown in Fig. 9.

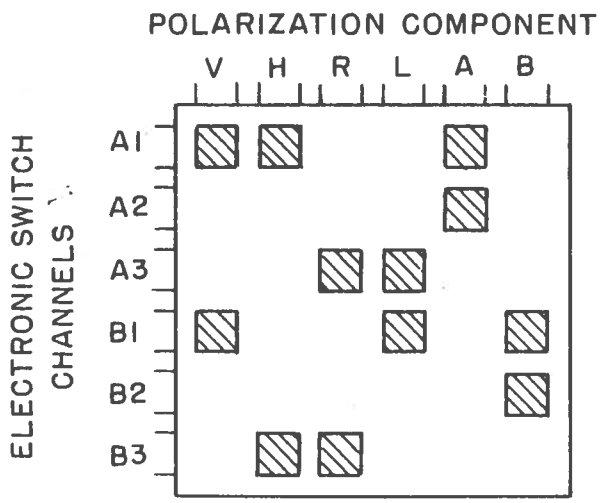


Figure 9 Electronic switch switching sequence

The logic circuit takes the six outputs of the commutator, buffers them, and feeds them to the required gates. The circuit uses RTL digital integrated circuits. Switch A1 is used as an example (see logic circuit in Fig. 8). The output of the first NOR gate will be low (0) whenever V, H, A, or ON is high (1) and the output of the second gate will be high. Thus the transistor will be off and its collector will be at -20 V. The 2-kΩ series resistance limits the current to the diode switch to 10 mA. When V, H, A, and ON are all low or the switch is in the OFF position, the output of the second NOR gate will be low. When this is so, the transistor is turned on and its collector is at approximately 4.0 V and the current supplied to the diode switch will be approximately 4 mA.

The manual switch (ON, AUTO, OFF) is a center-off DPDT switch. This allows each diode switch to be controlled separately and simplifies the setting up procedure of the electronic switch.

The Boolean function for each switch is given in Table II. When the function is zero, the switch is off.

TABLE II

Boolean functions for diode switches

$A1 = \overline{[OFF + \overline{(V + H + A + ON)}]}$	$B1 = \overline{[OFF + \overline{(V + L + B + ON)}]}$
$A2 = \overline{[OFF + \overline{(A + ON)}]}$	$B2 = \overline{[OFF + \overline{(B + ON)}]}$
$A3 = \overline{[OFF + \overline{(R + L + ON)}]}$	$B3 = \overline{[OFF + \overline{(H + R + ON)}]}$

The outputs of the diode switches are applied to a power divider used in the reverse mode. The power divider in this mode is a vector adder with an insertion loss of less than 1 db.

The IF Amplifiers

Two IF amplifiers are normally used in the polarimeter. The bandwidths available are 10 kHz and 20 kHz. The input signal is mixed with a 10.245-kHz oscillator signal to produce 455 kHz. The schematic diagram is shown in Fig. 10.

The mixer stage uses a tetrode N-channel field effect transistor. The local oscillator is isolated from each IF amplifier by a FET cascode stage to prevent interaction between the IF amplifiers.

There is one stage of amplification at 455 kHz. This is a FET cascode stage and a source follower circuit provides the necessary low-impedance input to drive the detector. The amplifier has a gain of greater than 60 db.

A 3-decade square law detector [2] is used. The response time of this extended range detector is limited only by the diodes and the time constant of the associated circuits. An operational amplifier amplifies the detected signal and also gives a low output impedance. The output of the detector follows the square law to about +8 V. The dynamic range of the signal is limited by the automatic attenuator so that the detector output does not exceed 2.0 V.

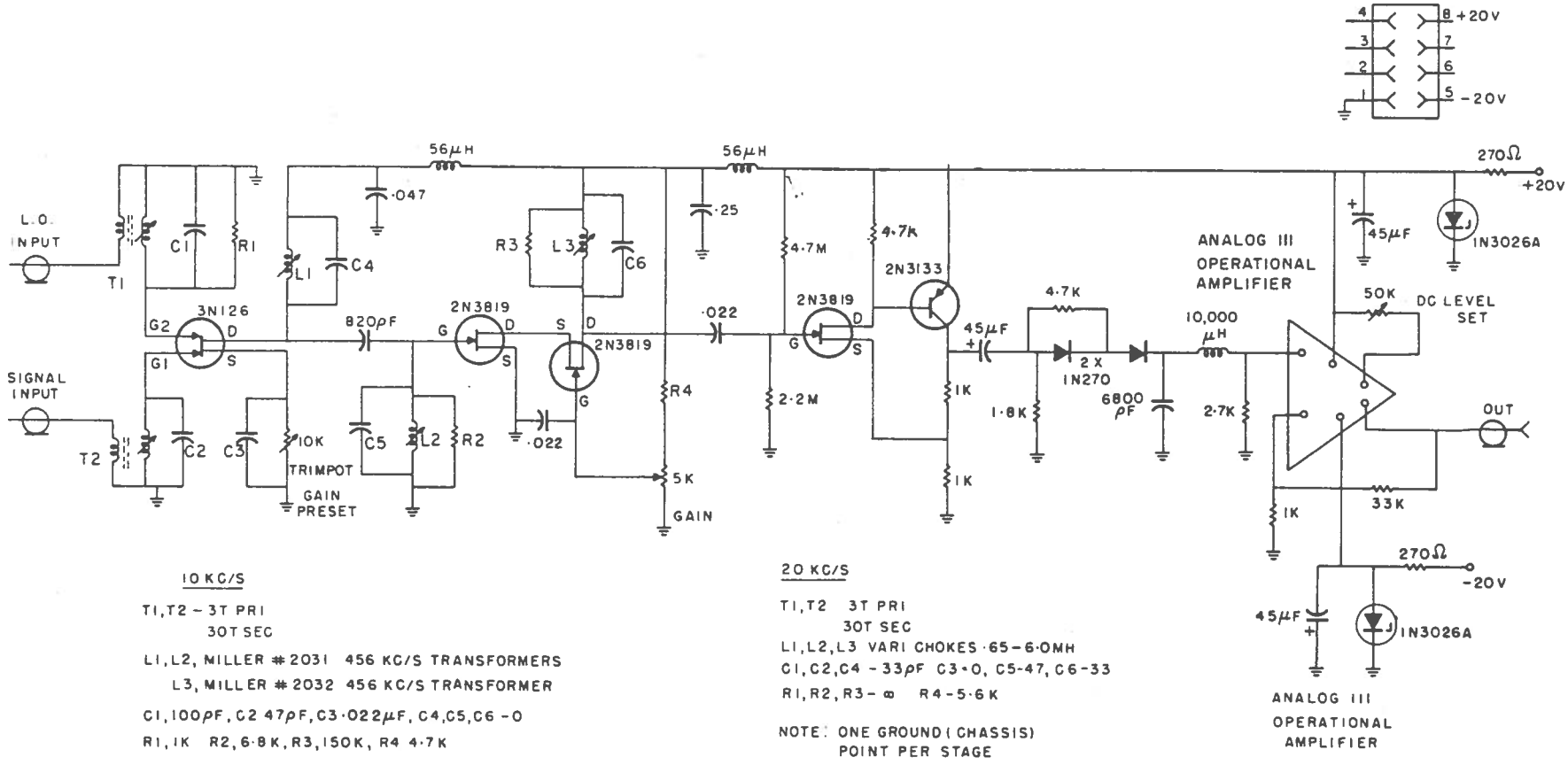


Figure 10 IF amplifier schematic diagram

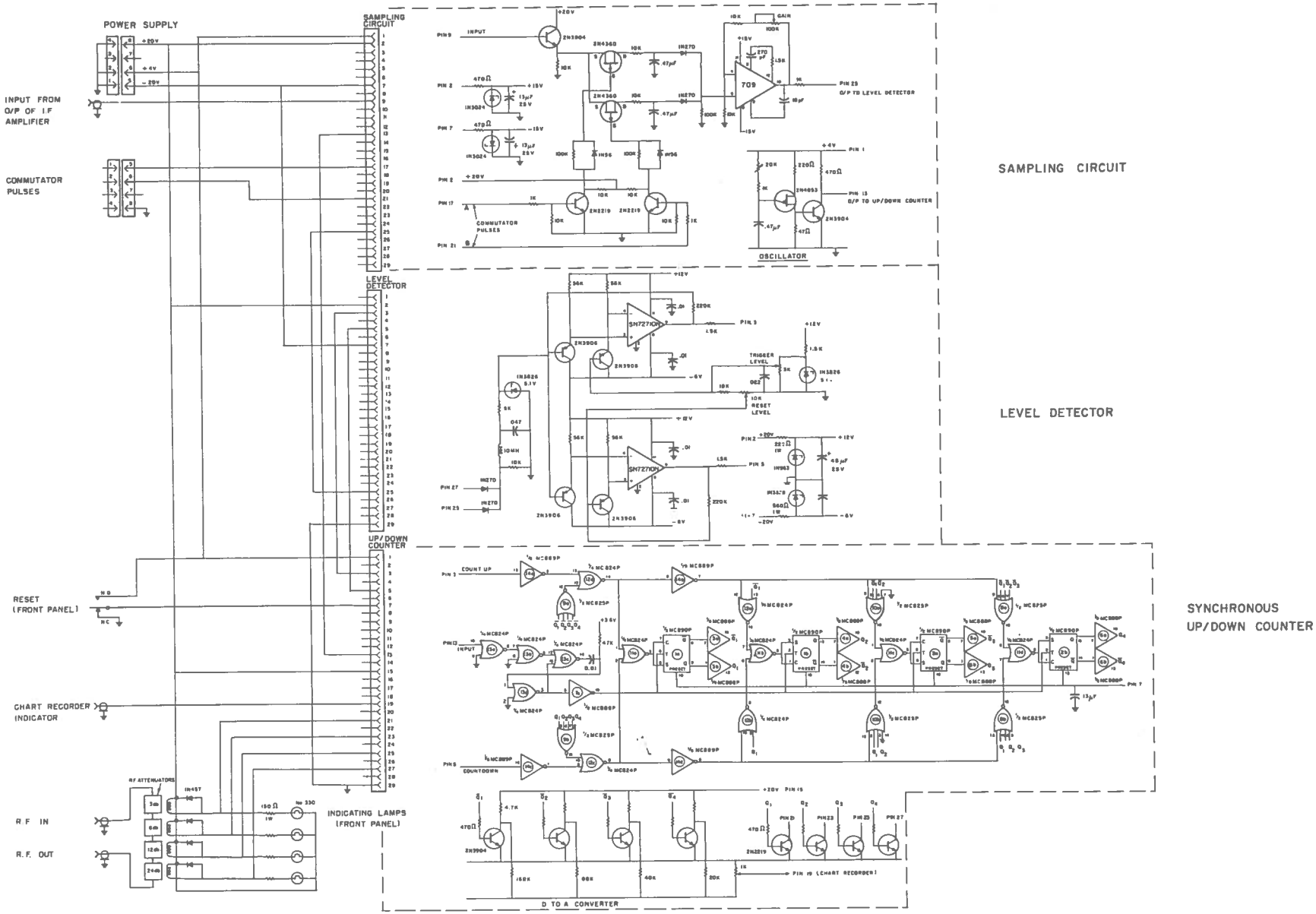


Figure 11 Automatic attenuator schematic

The Automatic Attenuator

When the output of the wide-band IF amplifier goes above (or below) preset levels, the automatic attenuator circuit inserts (or removes) attenuation that is common to both IF amplifiers. Four attenuators provide a range of 45 db in steps of 3 db. The circuit, shown in Fig. 11, can be broken down into four basic parts, the RF attenuators, the sampling circuit, the level detection circuit, and the up/down counter.

The RF Attenuators

The RF attenuator, shown in Fig. 12, is a coaxial structure with a low VSWR below 100 MHz. Coils mounted on the ends of the attenuator operate the reed switches.

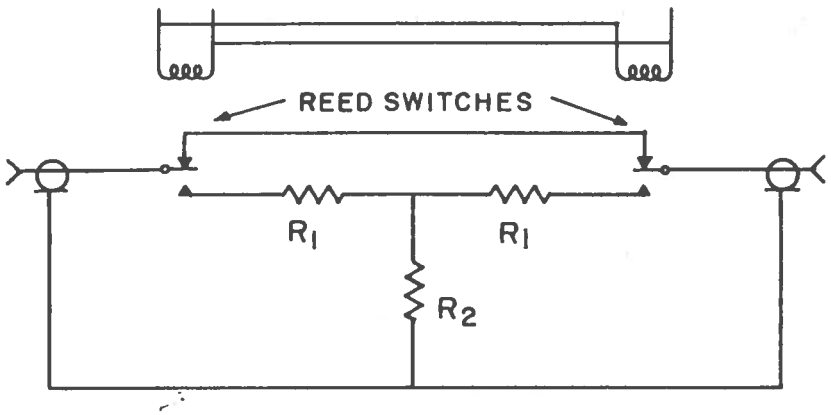


Figure 12 RF attenuator

The switching time is approximately 1 msec. The attenuators have attenuations of 3,6, 12, and 24 db. The attenuation network is an unbalanced T and the resistance values for the attenuators are given in Table III.

TABLE III

Value of resistances for constant impedance T section attenuator

Attenuation (db)	R1 (Ω)	R2 (Ω)
3	8.55	142
6	16.6	67
12	29.9	26.8
24	44.1	6.34

The Sampling Circuit

This circuit samples the output channels A and B of the wideband IF amplifier. There are two FET gates, one that is turned on when commutator pulse A is present and the other when pulse B is present. Each signal is then filtered, with a time constant of 5 msec.

The greater of the two signals is amplified by an operational amplifier. The gain of the operational amplifier is adjusted to give unity gain for the sampling circuit for a fixed dc signal input.

Also located on the same printed circuit card is a unijunction oscillator. The pulse output of the oscillator is used as the clock input to the up/down counter. The frequency of the oscillator is approximately 200 Hz.

The Level Detector

The function of the level detector is to give an output pulse whenever the signal from the sampling circuit goes above or below preset voltages. There are two preset voltages that determine when the circuit will operate. The trigger level potentiometer sets a voltage level (usually 2 V) above which the circuit inserts attenuation in the system. The reset voltage level, which is a fraction of the trigger level voltage (usually 0.5 V), determines when the circuit will remove attenuation.

At this point, it should be noted that the attenuators are located in the system before the IF amplifiers, and the input signal for the automatic attenuator is taken from the output of the IF amplifier. Thus when 3-db attenuation is inserted, the input signal to the level detector will be reduced by 3 db.

The level detector uses two integrated circuit comparators whose inputs are isolated by emitter followers. Since the maximum allowed input voltage to the comparators is ±5 V, the input voltage is limited by a zener diode.

The trigger level voltage is applied to the inverting input of one of the comparators and the input signal is applied to its non-inverting input. This comparator will have an output voltage of 0 when the input voltage is below the trigger level voltage. When the input voltage exceeds the trigger level voltage, the output voltage will be 4 V. There is dc positive feedback to increase the switching time of the comparator. This feedback introduces some hysteresis but this is not important in this application. The output of this comparator feeds the count-up bus of the up/down counter.

The input signals of the reset comparator are reversed, compared to those of the other comparator. That is, the reset voltage level is applied to the inverting input. The circuit operation is similar to the other comparator except that the output will be reversed. Thus, when the input signal is below the reset level, the output will be +4 V and when it is above, the output will be 0 V. The output of this comparator feeds the count-down bus of the up/down counter.

Up/Down Counter

The function of the up/down counter is to store the difference in the number of pulses on its two input lines. The output of each flip-flop controls one of the RF attenuators.

The JK flip-flops are normally held in the inhibit mode (SET and CLEAR inputs in the logic 1 state) to prevent false triggering. The flip-flops will change state whenever SET and CLEAR inputs are low and a negative-going transition is applied to the toggle input. The toggle signal is the output of a monostable multivibrator (NOR gates 13c and 13d in Fig. 11) whose input is the pulse from the unijunction oscillator on the sampling circuit card. Most of the circuit is made up of logic gates that enable the counter to count up and down. Two 4-input gates (9b and 9a) prevent the counter from counting below 0 and above 15.

The preset inputs of the JK flip-flops can be controlled at the front panel. When this line is low (logic 0 state), the counter operates normally. If the line is high (logic 1 state), the flip-flops are reset to their logic 0 state (Q is 0). This switch, if put in the logic 1 state, prevents the circuit from operating. The Q outputs of the flip-flops control transistors that in turn control the attenuators and indicating lamps on the front panel. The $\overline{Q}$ outputs control transistors that feed a resistive ladder network. The output of this D to A converter is fed to the chart recorder as an indication of the amount of attenuation in the system.

The Time Demodulator

The time demodulator synchronously detects the output of the square-law detector relative to the electronic switch. The outputs of the time demodulator are the six polarization components V, H, R, L, A, and B. The chassis contains six identical cards, each of which has two FET gates, a filter, and a dc amplifier. The block diagram is shown in Fig. 13 and the schematic diagram in Fig. 14.

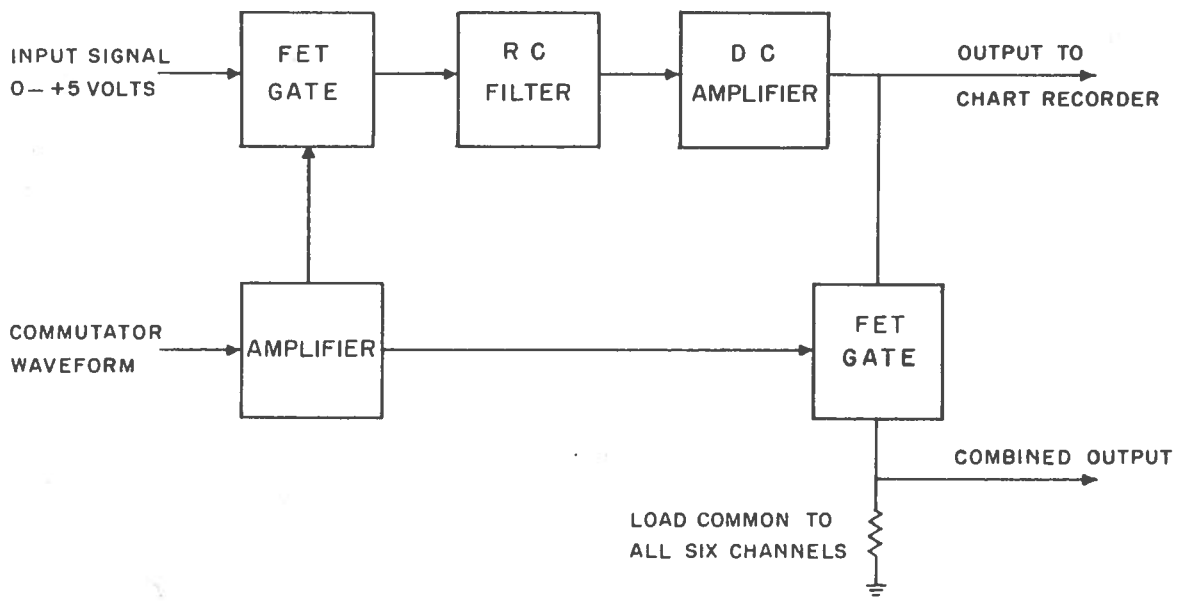


Figure 13 Block diagram of a time demodulator card

One of the FET gates samples the detected IF signal and the other samples the output of the time demodulator card. The second FET gate on each of the cards feeds a common

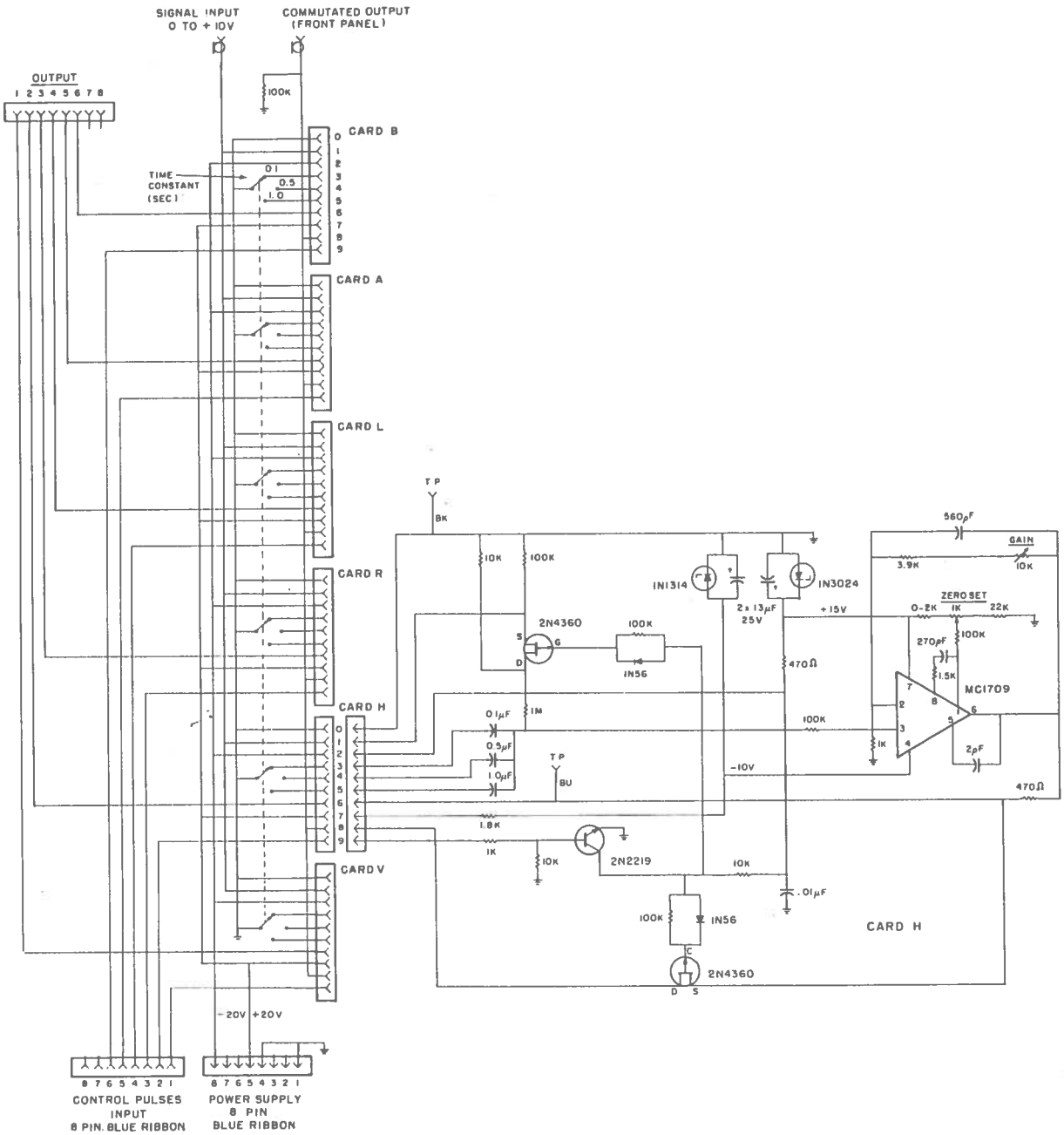


Figure 14 Schematic of the time demodulator

load resistor. The resulting waveform is a filtered version of the IF waveform and is very useful in setting up the polarimeter.

The FET gates are both controlled by the commutator. The commutator pulses are phase inverted and amplified by a common emitter stage on each card, and this waveform

is applied through decoupling networks to the gate terminals of the FET. When the voltage on the gate of the FET is +20 V, the FET is turned off. It then looks like a large resistance and the voltage developed across the 10-kΩ load resistor is zero. When the voltage on the gate is 0 V the FET is turned on. It then looks like a small resistance (approximately 500 Ω) and most of the input voltage is dropped across the load resistor. The error resulting from the ON resistance of the FET is less than 5% and is eliminated by adjustment of the gain of the dc amplifier.

The filter is a simple RC type with three time constants available. Any one of the three time constants, 0.1, 0.5, and 1.0 sec, may be chosen by grounding the required capacitor. This is accomplished by one switch that selects the required capacitor for each of the six channels.

A monolithic integrated-circuit operational amplifier is used as a dc amplifier. The amplifier has a gain of approximately 10, but the over-all circuit gain is unity. Gain controls allow the gain of the six channels to be made identical. A zero set control is available to reduce the output offset voltage to zero. The low impedance output used to feed the chart recorder is protected against short circuits.

APPENDIX

Antenna Description

The antenna is oriented in relation to the direction of propagation and the celestial meridian as illustrated in Fig. 15. With the antenna elements A and B connected to the correspondingly labeled inputs of the polarimeter, the circular polarization components, R and L, have the senses of rotation as described in the IRE standards (1942). The antenna elements are positioned ±45° to the celestial meridian. This provides a reference for describing the orientation angle of a polarized wave.

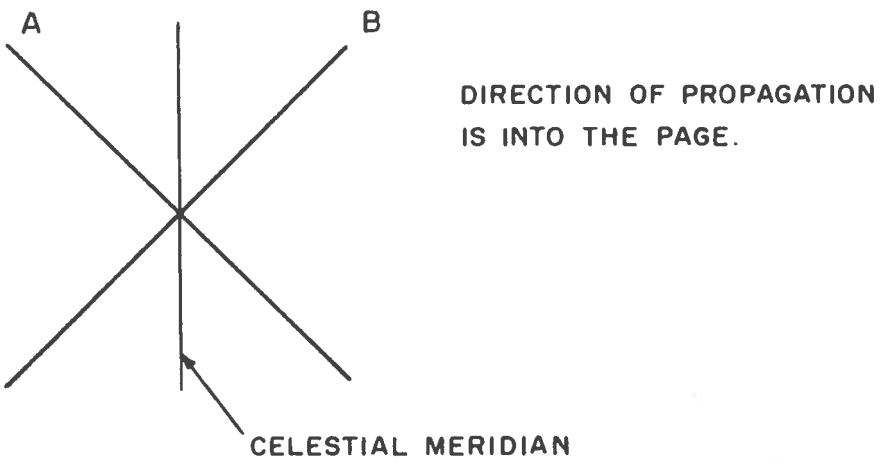


Figure 15 Description of antenna

Initial Set-up Procedure

This procedure is followed when the polarimeter is moved or has been turned off for a long period of time.

The noise diode calibration circuit has to be adjusted for the correct current levels. A digital voltmeter should be used to measure the voltage across the 200-Ω sensing resistor for noise diode A. The trimming potentiometers associated with the transistor switches are adjusted to give the desired voltage. The potentiometer in the summing network of error detector B is adjusted to give equal voltages for noise diode B.

The bandpass and center frequencies of the RF and IF amplifiers are adjusted. Also the preset gains are adjusted (internal adjustment) for the approximate operating range.

The setting up procedure for the electronic switch is very easy if a vector voltmeter is available. A 10.7-MHz signal is applied through a power divider to both inputs. The reference probe of the vector voltmeter is connected at the power divider and the other probe is connected at the output of the chassis. With diode switch A1 on and the other switches off, the signal generator is adjusted to give 10 mV at the output of the chassis, and the phase offset of the vector voltmeter is adjusted to read 0°. Then diode switch A1 is turned off and A2 is turned on. The controls of channel A2 are adjusted to give an output of 4.1 mV and a phase of 0° relative to channel A1. The remaining channels are set up in a similar manner. The relative settings are given in Table IV.

TABLE IV

Relative settings of electronic switch channels

Channel	Amplitude	Phase
A1	10 mV	0°
A2	4.1 mV	0°
A3	10 mV	90°
B1	10 mV	0°
B2	4.1 mV	0°
B3	10 mV	180°

Five controls in the automatic attenuator need adjustment. The unijunction oscillator is set for a period of 5 msec. The sampling circuit should be adjusted for unity gain. The trigger and reset voltage levels are adjusted for the type of output recorder used. For an instrumentation tape recorder, whose linear voltage range in the FM mode is +2.5 V, the trigger level is set so that attenuation is inserted when either channel A or B is 2.0 V. The reset level is adjusted so that when channels A and B go below 0.5 V, attenuation is removed. The amplitude of the output of the digital/analog converter is adjusted to give a convenient indication on the chart recorder.

Routine Set-up Procedure

This procedure is followed whenever necessary. Normally, once a week is sufficient.

The first step is to adjust the chart recorders and tape recorder independently of the system. The commutator frequency control is then adjusted to give a sampling period of 5 msec.

The time demodulator is the next chassis to be adjusted. The input of the chassis is grounded and with an oscilloscope connected to the output of one of the printed circuit cards, the zero-set potentiometer is adjusted to give a zero output (to within ±10 mV). A dc voltage (+3 V, approximately) is applied to the input and, using the subtraction feature of a dual-channel oscilloscope, the gain control on the printed circuit card is adjusted to give the same voltage (to within ±10 mV) as the input. This procedure is carried out for the remaining five cards.

To set up the RF amplifier, a 73.8-MHz signal is introduced through a power divider to the inputs of the amplifiers. The gains of RF amplifiers are made equal. By means of the phase shifter, the relative phase shift between the two amplifiers is adjusted to zero. The resulting output waveform is shown in Fig. 16. The gains of the RF amplifiers are then readjusted to give equal amplitudes on channels A and B for a noise diode current of 25 mA. The gains of the IF amplifiers are adjusted to give approximately 0.5 V at the outputs of the time demodulators for a noise diode current of 25 mA.

Figure 16 Combined output waveform for an equal amplitude coherent input signal

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2. Bose, C.C., Steppe, A., and Thacker, D. Power law detector. Proc. IEEE, 53: 2155; 1965.