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DIGITAL LIGHTHOUSE REMOTE - CONTROL

- F. VACHON -

OTTAWA
JANUARY 1969

DIGITAL LIGHTHOUSE REMOTE-CONTROL

by:

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Radio and Electrical Engineering Division AVALVZED
National Research Council

CANADA

SUMMARY

Eight latching relays may be turned on or off at each of eight different locations by one transmitter. Integrated circuits are used for 90% of the logic circuitry. A general description, including block diagrams, is given in this paper.

DIGITAL LIGHTHOUSE REMOTE-CONTROL

INTRODUCTION

This digital system was designed to turn lighthouse equipment ON or OFF remotely by a radio link. Eight latching relays may be operated at each of eight different locations by one transmitter. The logic circuitry is about 90 percent integrated circuits and 10 percent discrete components.

A telemetry system is being considered to monitor the remote control operations, but this paper deals only with the remote control function.

DESCRIPTION OF TRANSMITTING END

A 10-watt, 1792 KHz, laboratory-built transmitter was used in preliminary tests over a distance of seven miles. The transmitter was keyed on and off (modulated) by the logic circuitry shown in photograph #1 and #2, and in Fig. 1.

Typical modulation patterns are shown in Fig. 2.

Patterns (a) and (b) will turn ON and OFF relay No. 1 at location No. 1. As can be seen the patterns are composed of an endless series of 8-bit words. The words of one pattern are all identical except for the first bit of each word. This is a sync bit which alternates between a "1"

and a "0" (zero). A "1" turns the transmitter on and a "0" turns it off. The second, third and fourth bits indicate the location number and are selected by turning an eight-position switch to the desired location. The fifth bit indicates that the relay is to be turned ON if it is a "1" and OFF if it is a "0". This bit is selected by push-buttons. The last three bits indicate the relay number and are again selected by an eight-position switch.

When none of the push-buttons are depressed, a modulation pattern is produced as shown in Fig. 2(c). This pattern (idling pattern) cannot operate any relays. It is transmitted to keep the power on and to maintain bit-timing at the receiving end between commands. If the ON push-button is depressed the pattern changes from (c) to (b), (if location 1, relay 1, has been selected). If the OFF pushbutton is depressed the pattern changes to (a).

The shift register is shifted every 140 µsecs by a crystal-controlled clock. After 8 shifts the register contains all 0's regardless of what was initially in it. Therefore, only the 1's of any code word need to be loaded, every 1120 µsecs (every word), into the appropriate flipflops as determined by the switches. Loading pulses are produced by dividing the shift pulses by 8. A further division by 2 provides pulses every 2240 µsecs. to load a "1" into the output flip-flop only on every second word.

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DESCRIPTION OF RECEIVING END

A 1792 KHz, laboratory-built receiver was used. The intermediate frequency of the receiver (455 KHz) is detected and sliced. Detector output turns the power on for the logic circuitry (shown in photograph #3 and #4, and Fig. 3) and signal slicer. When no signal is being received the only battery drain in the logic circuitry is 50 μ a from the 6-volt battery.

Bit sampling and bit-timing recovery

Each bit (140 µsecs duration) of the command is sampled 5 times at 20 µsecs intervals for more dependability. This sampling has to be properly phased with the incoming bits so that all 5 samples are taken during the 140 µsecs allotted for each bit.

The sliced waveform is used to condition an auxiliary 5-bit shift register which is shifted every 20 µsecs by a crystal-controlled clock so that each bit is actually sampled 7 times. Only five of these samples are retained in the shift register. Summing resistors (adder) and a Schmitt trigger give an output which depends on whether the majority of samples are 1's or 0's. The Schmitt output is compared with the first and last flip-flops of the 5-bit register. If all three are the same, the divide by 7 counter is undisturbed. However, if one of the flip-flops is different from the Schmitt, it is because the 5 samples were taken

partly before and partly after a transition in the code. The divide by 7 counter will then be gated in such a way as to speed up or slow down by one count (20 μ secs) in an effort to position all 5 samples on the same side of a transition. If it is not successful the first time, the counter will speed up or slow down again at the next transition. A maximum of 2 transitions are required to properly position the 5 samples.

The Schmitt output is also used to condition the main shift register which is shifted every 140 $\mu secs$ by the output of the divide by 7 counter.

Main shift-register and hold-register

The main shift-register has 9 flip-flops and the first is compared with the last. With this arrangement, all the bits of one word are compared with the corresponding bits of the next word. The comparator produces a pulse when 2 bits are different (like 2 sync bits). This pulse initiates a delay (counter type) which produces another pulse after 1120 μ secs (1 word time), provided the delay is not reinitiated before the 1120 μ secs are over.

The delayed pulse is gated with the next comparator pulse and the 3 location bits in the shift-register. This produces a loading pulse for the 4-bit hold-register provided the location bits are correct for that particular location. The hold-register is held at 0000 until 4

consecutive loading pulses have been produced. On the fourth and every succeeding loading pulses the hold-register will be loaded with the transmitted command until the loading pulse is missed. When a pulse is missed the register will return to 0000 until another 4 consecutive loading pulses are produced.

The four-bit hold-register is then decoded by 8 gates and 2 transistor switches to produce the 16 possible outputs. These are connected to the coils of 8 latching relays to turn them ON or OFF. An extra input was provided on the gate for the number 1 relay to prevent it from being enabled when no loading pulses are produced and the hold-register is at 0000.

CONCLUSION

The preliminary tests over a radio link have been very encouraging. The percentage of successful transmissions approaches 100 percent with no false operations. Reliable operation was achieved even in the presence of appreciable noise pulses from other radio signals.

Although designed with lighthouse control in mind, this system might be used for any other application where remote ON and OFF functions are required.

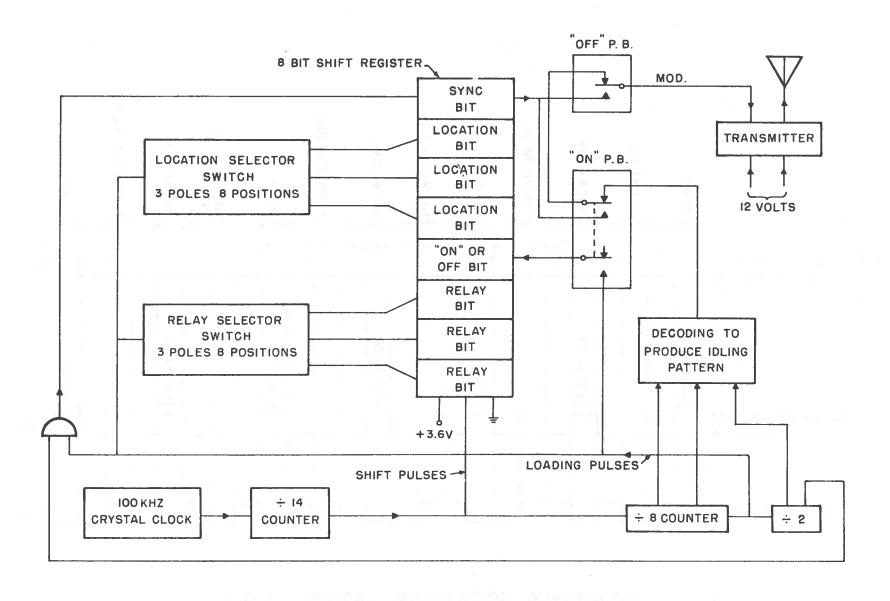


FIG. I - BLOCK DIAGRAM - TRANSMITTING END

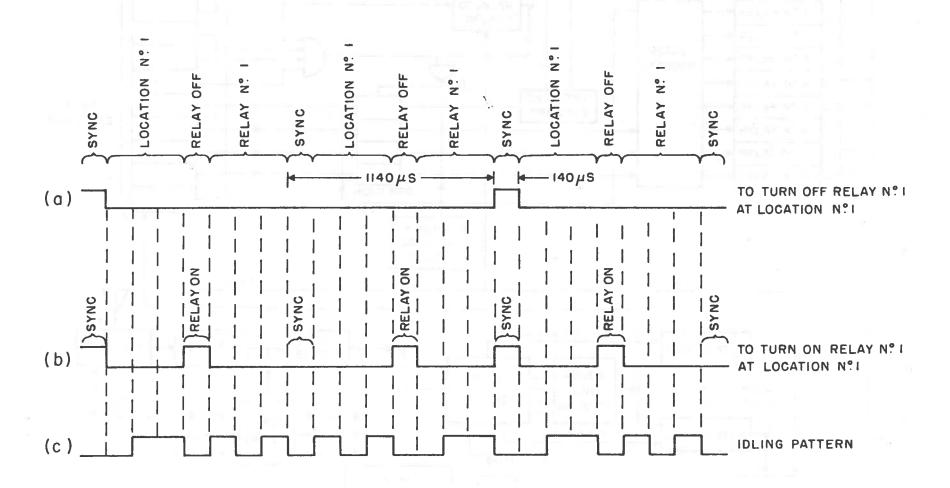


FIG. 2 _ TYPICAL MODULATION WAVEFORMS

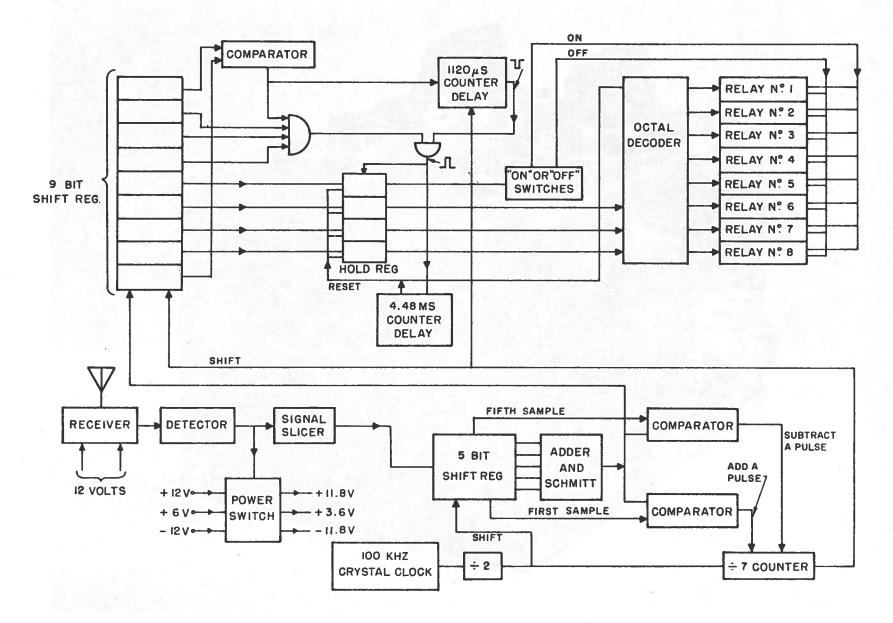
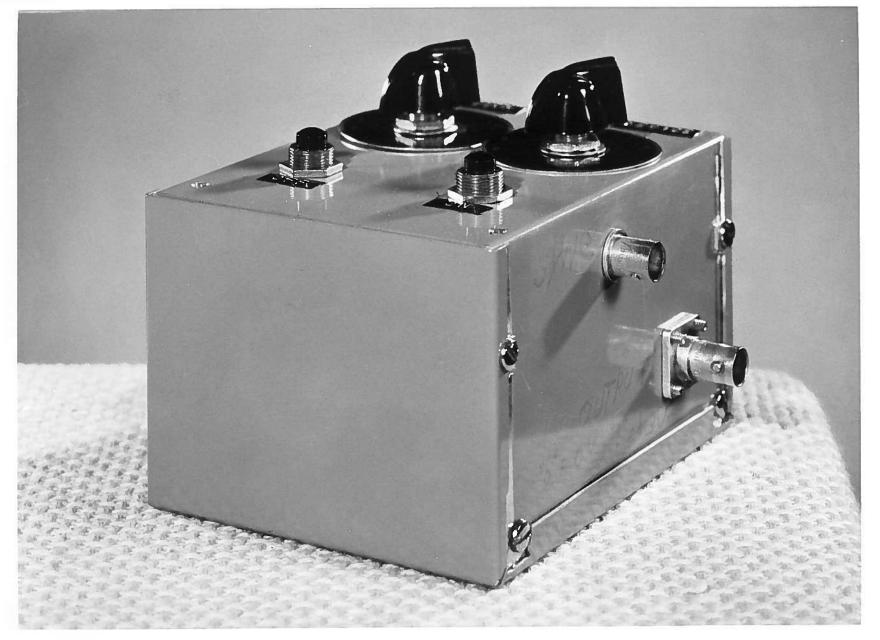
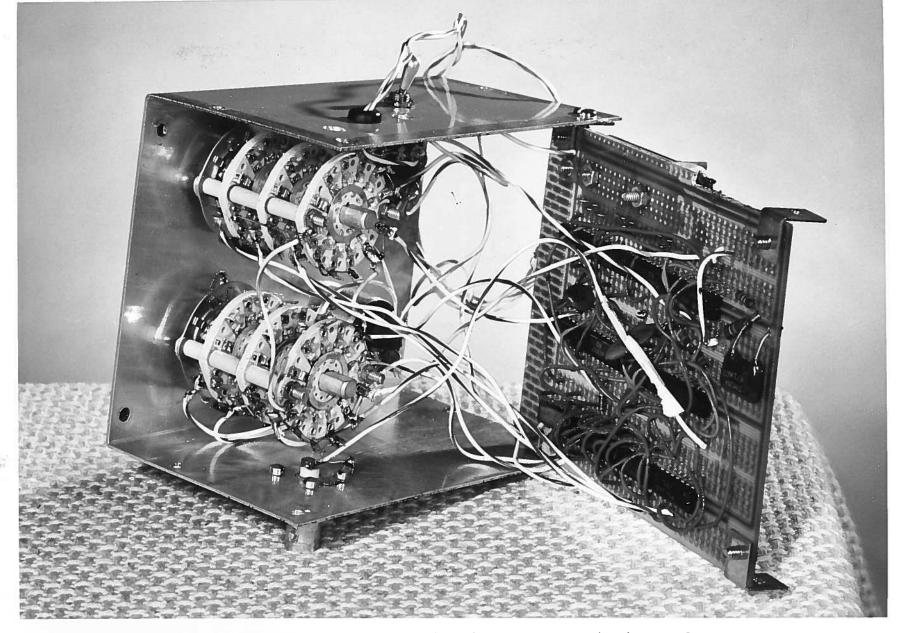


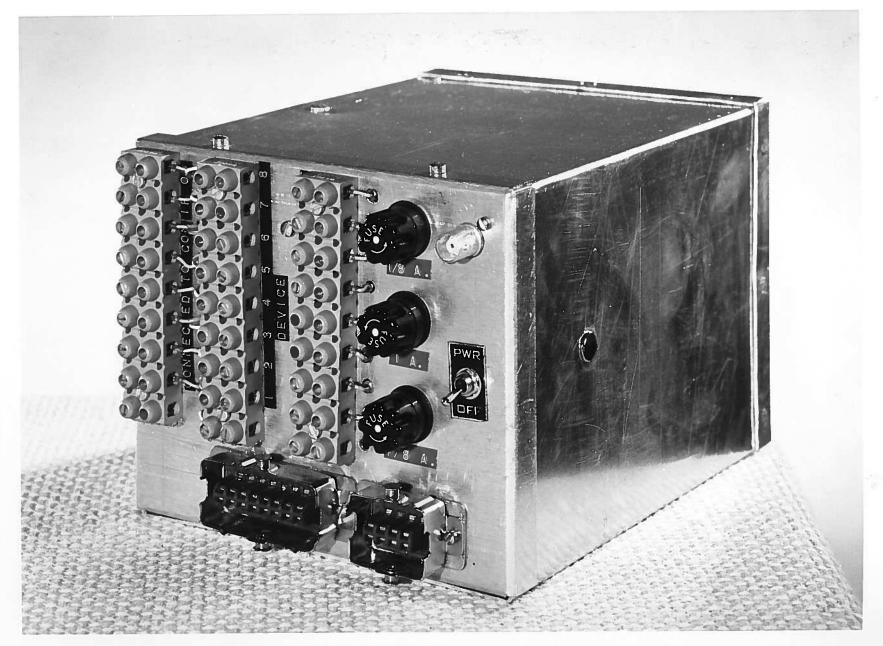
FIG. 3 - BLOCK DIAGRAM - RECEIVING END



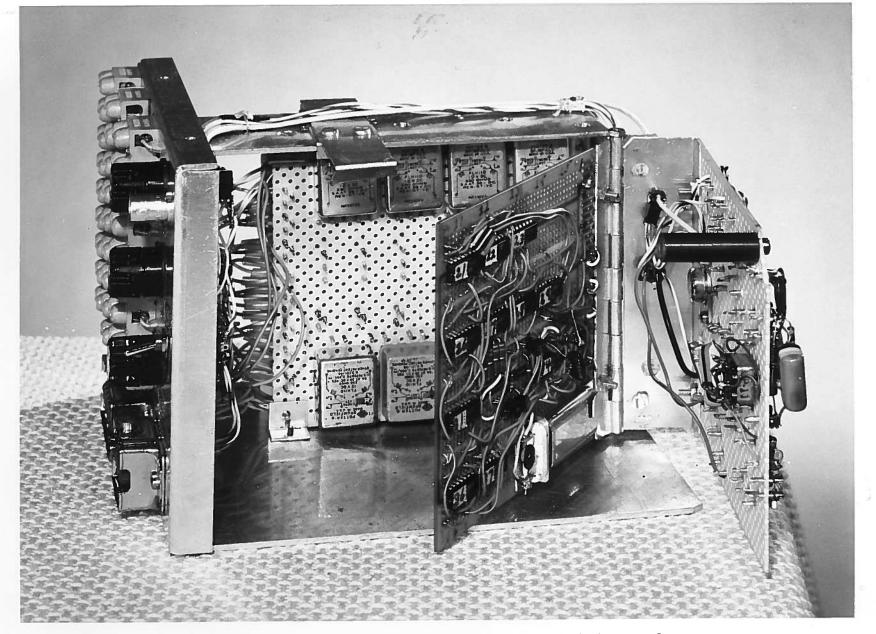
Photograph #1 - Logic Circuitry - transmitting end.



Photograph #2 - Logic Circuitry - transmitting end



Photograph #3 - Logic Circuitry - receiving end



Photograph #4 - Logic Circuitry - receiving end