A frequency divider from 100 kilocycles/second to 60 cycles/second

Makow, D.

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H. Foss Smyth

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RADIO AND ELECTRICAL ENGINEERINIG DIVISION

A FREQUENCY DIVIDER FROM 100 KILOCYCLES/SECOND TO 60 CYCLES/SECOND

D. MAKOW

OTTAWA

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ABSTRACT

A chain of frequency dividers from 100 kilocycles/second to 60 cycles/second employing regenerative modulation is described. Simplified and stable dividers have been developed which permit a reduction of the number of circuit components and the size and weight of the chassis. Operation of the system is maintained through considerable variation in the input, plate, and filament voltages, or frequency of the input.

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A FREQUENCY DIVIDER FROM 100 KILOCYCLES/SECOND TO 60 CYCLES/SECOND

- D. Makow -

INTRODUCTION

A voltage of known and constant frequency is very useful as a reference in time and frequency measurements. The frequency of a temperature stabilized crystal-controlled generator has high stability and is suitable for this purpose. The highest stability of such an oscillator is realized in the region of 100 kilocycles/second, where quartz crystals have optimum properties. Frequency multipliers and dividers can extend the application of such a frequency standard into the desired frequency regions. Often a low-frequency component derived in this manner is employed to drive a clock, which is used as an accurate time indicator and can serve also as a means of comparison with the time signal transmitted by distant frequency standard establishments.

The present paper describes a chain of frequency dividers from 100 kilocycles/second to 60 cycles/second. Dividers employing regenerative modulation [5] are more reliable than those of the locked oscillator or multivibrator type, since no self-oscillation can take place when the controlling frequency fails. They have been used recently in a number of other frequency standard installations [1], [2], [3], [6]. In the system to be described, the number of circuit elements and the space needed for a divider chain of this type have been reduced. A simplified and stable divider for the ratio ten-to-one has been developed and employed in the first two stages of the divider chain. Another type of divider [4] which permits the use of small low-Q inductors instead of the voluminous low-frequency coils currently utilized at low frequencies, has been employed in the last stage of the divider chain.

DESCRIPTION

PERFORMANCE CHARACTERISTICS OF THE REQUIRED SYSTEM

In the frequency standard installation of the National Research Council a system of frequency dividers is required, capable of generating 2-milliwatt signals at frequencies of 10 and 1 kilocycles/second, and 100 and 60 cycles/second, and controlled by a 100-kilocycle high stability crystal oscillator. These frequency components are useful as standards in the laboratory. The 60-cycle/second signal, in particular, is required to drive a clock. The operation of the divider stages should not be influenced by power supply and input voltage variation or by drift in the values of circuit elements and in the absence of the input signal no output signals should be generated. Light weight and small size of the chassis is one desirable feature of the equipment.

TYPES OF FREQUENCY DIVIDERS EMPLOYED

Frequency dividers employing regenerative modulation fulfill the requirement of stable frequency division unusually well, and they were chosen for all stages of the system.

As a basis of the design two types of frequency dividers employing regenerative modulation were planned. The first type uses the principle described in Ref. 5 and was developed for the division ratio of 10:1. The operation of this divider is as follows (see Fig. 1).

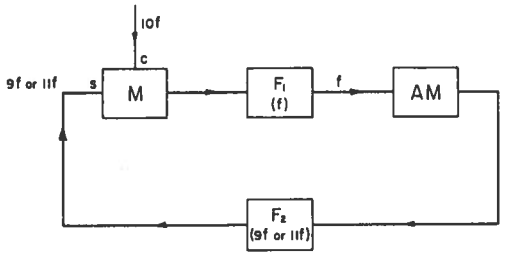


FIG. 1 BLOCK DIAGRAM OF FREQUENCY DIVIDER EMPLOYING REGENERATIVE MODULATION

DIVISION RATIO 10:1

The input frequency $10f$ is applied to the carrier input c and the signal frequency $9f$ or $11f$ is applied to the signal input s of the balanced ring modulator M . The difference frequency f present among the modulation products of M is passed by the filter F_1, centered at this frequency, and is applied to an amplifier and frequency multiplier AM where the required power at the ninth or the eleventh harmonic of f is obtained. This signal is then passed by the filter F_2, centered at $9f$ or $11f$, and is then applied to the input s of M, providing the initially assumed frequencies $9f$ or $11f$. It is seen that operation is possible when either the ninth or the eleventh harmonic is chosen. The ninth or the eleventh harmonic can be made available, in addition to the frequency f at the output of this divider.

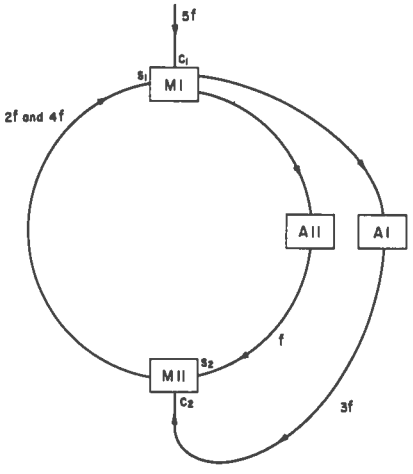


FIG. 2 BLOCK DIAGRAM OF FREQUENCY DIVIDER EMPLOYING REGENERATIVE MODULATION

DIVISION RATIOS 5:3 AND 5:1

The second type of frequency divider is described in Ref. 4 and has been developed to generate the fractional frequencies f and $3f$ from the input frequency $5f$. The operation of this divider is as follows (see Fig. 2). The input frequency $5f$ is applied to the carrier input c_1 and the signal frequencies $2f$ and $4f$ are applied to the signal input s_1 of the balanced ring modulator MI . The difference frequencies f and $3f$ present among the modulation products of MI are amplified in tuned amplifiers AII and AI , respectively, and are then applied to the inputs s_2 and c_2 of the balanced ring modulator MII . The difference frequency $2f$ and the sum frequency $4f$ found among the modulation products of MII are applied to the signal input s_1 of MI , thus providing the initially assumed components. This circuit generates the odd and the even fractional frequencies at separate output terminals and delivers the frequencies f and $3f$ at usable power levels.

A SYSTEM DESIGN WITHOUT LOW-FREQUENCY CIRCUITS

Some work was done investigating the possibility of eliminating the voluminous low-frequency coils required for the last two divider stages of a chain. A system shown in Fig. 3 was devised but not realized, which avoids the need for operation in the low-frequency ranges, and takes advantage of the properties of the two types of frequency dividers described above. The dividers DI, DII, and DIII operate as explained with reference to Fig. 1. DI divides the 100,000 cycles/second input by ten, supplying 10,000 cycles/second signals for the Output I of the system, for the input of DII , and for the input of the mixer MI ; DII divides the 10,000 cycles/second input by ten, supplying 1000 cycles/second signals for the Output II of the system and the amplifier-multiplier unit AM , and a 9000 cycles/second signal for the input of the divider DIII . DIII generates eleven-tenths of its input frequency, namely 9900 cycles/second for the input of DIV and for the input of the mixer M_1 . The mixer generates the frequency of 100 cycles/second as a difference of its two input frequencies, which are 10,000 cycles/second and 9900 cycles/second. The output frequency components of the balanced mixer MI are given by

$$n \cdot 10{,}000 \text{ c/s} \pm 9900 \text{ c/s}, \quad n = 1, 3, 5, \ldots\ldots$$

and they are all, except for the usable frequency of 100 cycles/second, higher than 9900 cycles/second. Therefore the filter FI may be of the low-pass type which cuts off below 9900 cycles/second. The divider DIV being of the type shown in Fig. 2, provides the mixer MII with three-fifths of its input frequency, that is, with 5940 cycles/second. The mixer MII generates a 60 cycles/second frequency component as a difference frequency of 6000 cycles/second and 5940 cycles/second, the former being the sixth harmonic of 1000 cycles/second produced by the amplifier-multiplier unit AM . Similarly to the filter FI the filter FII can be of the low-pass type and has a cut-off frequency below 5940 cycles/second.

It is seen that all elements of this system operate in the kilocycle frequency region where the realizable Q values of the resonant circuits are high and the size of the elements

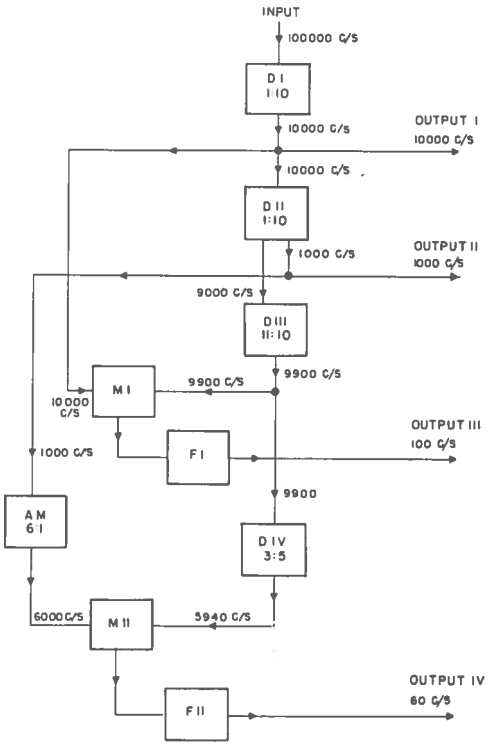


FIG. 3 BLOCK DIAGRAM OF DIVIDER CHAIN FOR GENERATION OF 10 KC/S, 1 KC/S, 100 C/S, AND 60 C/S SIGNALS WITHOUT EMPLOYING LOW-FREQUENCY CIRCUITS

is small. However, it has been found during the development of this system that the stability of the frequency divider shown in Fig. 1, when utilizing the eleventh harmonic, is inferior to that when utilizing the ninth harmonic. Since the divider DIII supplies the subsequent stages at a frequency that is eleven-tenths of its input frequency, it would have to employ the eleventh instead of the ninth harmonic, and it would then become the weak point in the system. This deficiency could be overcome by generating the eleventh harmonic separately. However, this would result in an increased number of elements.

A SYSTEM DESIGN USING LOW-Q COILS IN DIVIDER STAGES FROM 1000 C/S TO 60 C/S

The inductors intended for use in the resonant circuits of the divider stages employ non-metallic ferromagnetic material known as "Ferroxcube". These are recommended for use in the frequency range from 1 kilocycle/second to 1 megacycle/second and higher, where high Q values are readily obtainable. At 60 cycles/second and 100 cycles/second values of Q of 4 and 7, respectively, were measured. Consideration has been given to the system shown in Fig. 4, where straight frequency division down to 60 cycles/second is employed and Ferroxcube inductors are also used for the last

two stages of the divider chain. In Fig. 4, DI and DII are dividers of the type shown in Fig. 1, generating 10 kilocycles/second and 1 kilocycle/second signals. DIII is also a divider stage of the same type, generating a 100 cycles/second signal. However, in this divider stage multiplication by nine takes place in two steps of three each, thus lowering the requirements imposed on the selectivity of the tuned circuits. Also, a frequency component of 300 cycles/second becomes available, which is used to drive

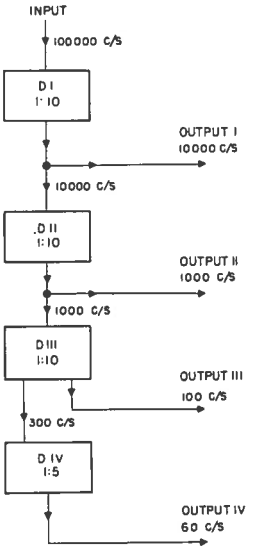


FIG. 4 BLOCK DIAGRAM OF DIVIDER CHAIN FOR GENERATION OF 10 KC/S, 1 KC/S, 100 C/S, AND 60 C/S SIGNALS WHICH EMPLOYS LOW-FREQUENCY CIRCUITS

the next stage. The divider DIV is of the type shown in Fig. 2, and it divides its input frequency of 300 cycles/second by five, generating the required frequency component of 60 cycles/second. The divider type shown in Fig. 2 was chosen for DIV in preference to the type shown in Fig. 1, since in the former case the useful component of 60 cycles/second is available separately at a relatively high power level, and the odd and even fractional frequencies are generated at separate output terminals, lowering the required selectivity of the tuned circuits.

An alternate solution for the design of stages DIII and DIV would employ division by ten for the former and division by five-thirds for the latter. The DIII stage would use the divider type shown in Fig. 1, and the DIV stage would use the divider type shown in Fig. 2, which is particularly suitable for this division ratio. The latter, however, would have to employ a circuit resonant at 20 cycles/second where the selectivity of Ferroxcube inductors decreases to the value Q = 2. This method of deriving a 60 cycle/

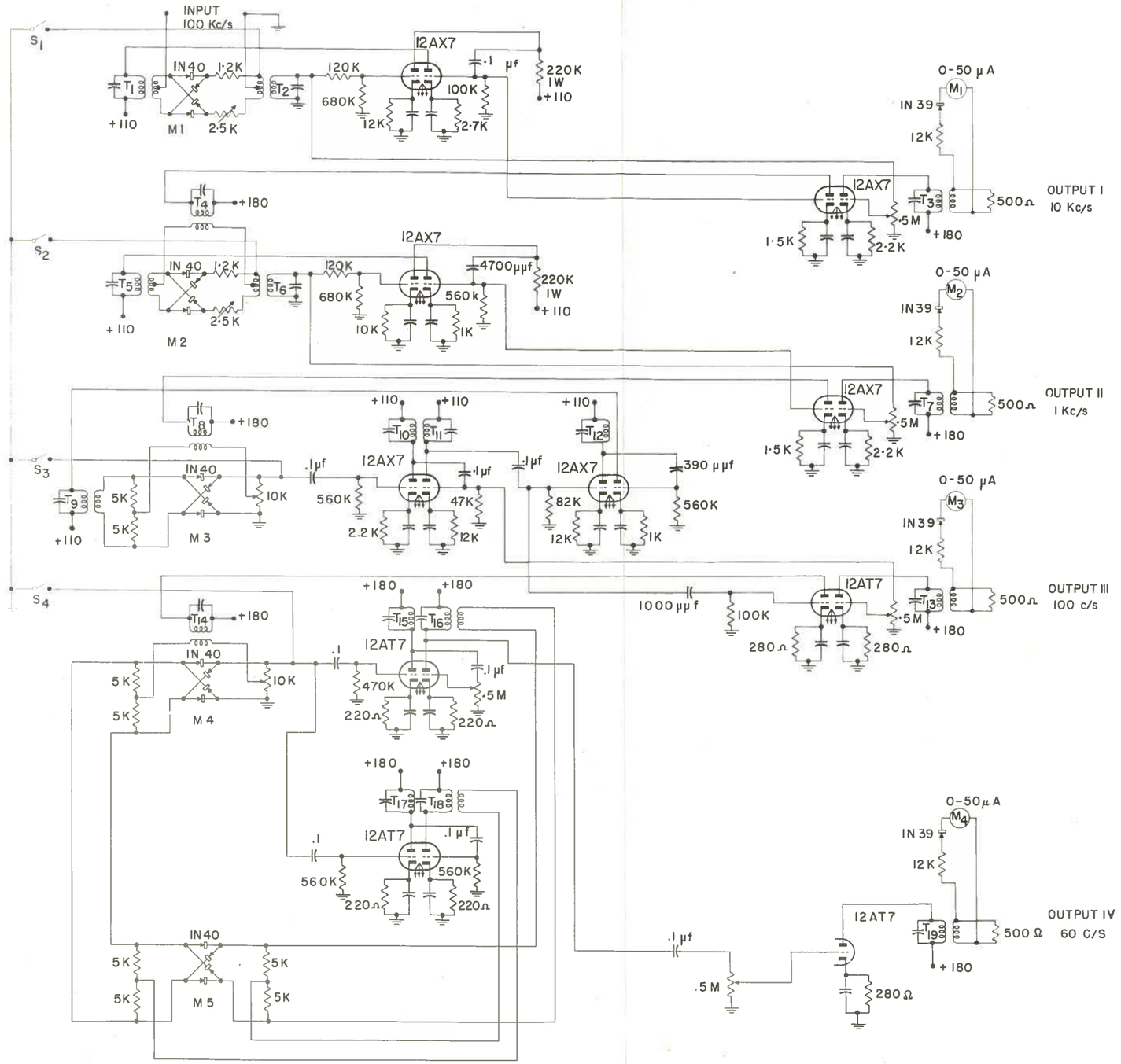
second component directly from a 100 cycles/second source is interesting, but since it would have to employ several tuned circuits to obtain the required selectivity at 20 cycles/second it has been abandoned in favour of the previous solution.

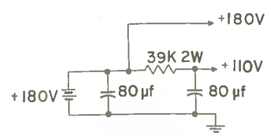
DETAILED DESCRIPTION OF THE SYSTEM DESIGN EMPLOYED

An estimate of the number of components used for the system shown in Fig. 4 compares favourably with the number used in the system shown in Fig. 3, and therefore it was decided to develop the former system. Fig. 5 shows the complete circuit diagram of the four divider stages. The first and the second divider stages are very similar. The 100 kilocycles/second signal is applied to the carrier input of a balanced ring modulator MI. The four matched germanium diodes (Sylvania type-1N40) are nearly equal in their characteristics. Additional balance can be obtained by means of a 2.5 kilo-ohm potentiometer. The tuned circuit T_1 resonates at 90 kilocycles/second and is coupled inductively to the ring modulator. The circuit T_2 is tuned to 10 kilocycles/second. In order to prevent generation of an undesired fractional frequency, e.g., 11, 111.1 cycles/second or 9090.9 cycles/second, which are 1/9 or 1/11 of the input frequency, respectively, the tuned circuits must introduce sufficient attenuation at these frequencies. It has been found experimentally that selectivity of the tuned circuit corresponding to a value of Q = 25 is adequate to assure satisfactory operation. The bias of the first triode section of the type-12AX7 tube has been chosen for maximum production of the ninth harmonic. The second triode section of that tube acts as a frequency multiplier, its plate circuit being tuned to a frequency of 90 kilocycles/second. Connections are made from the inputs of the first and second triode sections to the output stages, which employ a type-12AX7 double triode. The output stages supply a 2-milliwatt, 10 kilocycles /second signal to the 500-ohm output load and a 10 kilocycles/second carrier voltage for the ring modulator input of the second divider stage. The tuned transformers T_3 and T_4 provide additional frequency discrimination and match the low impedance loads to the plate resistance of the output stages. The circuit of the second divider stage, generating a 1 kilocycle/second output frequency, is similar to the preceding one. A small coupling capacitor of 4700 $\mu\mu$f between the two triode sections emphasizes amplification of the desired harmonic. The time constant of the R-C element has been chosen experimentally for satisfactory starting properties of the circuit.

The third divider stage generates a 100 cycles/second frequency component for the output load and a 300 cycles/second frequency component to drive the next divider stage. A resistance center-tap network, instead of the transformer type used for MI and M2, has been employed for the ring modulator M3 since it is simpler to provide at low frequencies. The 100 cycles/second frequency component of the ring modulator output is amplified in the first triode section of the first type-12AX7 tube, which is tuned to 100 cycles/second by means of the resonant circuit T_{10}. The second triode section is tuned to 300 cycles/second by means of the resonant circuit T_{11}. Both triode sections of the second type-12AX7 tube are tuned to 900 cycles/second by means of the resonant circuits T_{12} and T_9. The values of the cathode resistors and some of the

RESONANT CIRCUIT	RESONANT FREQUENCY	INDUCTORS (FERROXCUBE POT CORE AIR GAP .006 IN.) NUMBER OF TURNS PRIMARY	SECONDARY	WIRE Nos.	CAPACITORS CAPACITANCE VALUE
T_1	90 Kc/s	100	15 + 15	26	1000 µµf.
T_2	10 "	280	50 + 50	30	10000 µµf.
T_3	10 "	350	30	30	8200 µµf.
T_4	10 "	350	30	30	8200 µµf.
T_5	9 "	280	50+50	30	10000 µµf.
T_6	1 "	1000	150+150	36	.1 µf.
T_7	1 "	1200	100	36	.06 µf.
T_8	1 "	1200	100	36	.05 µf.
T_9	900 c/s	1000	300	36	.07 µf.
T_{10}	100 "	3000	-	39	.7 µf.
T_{11}	300 "	1300	-	36	.3 µf.
T_{12}	900 "	1300	-	36	.04 µf.
T_{13}	100 "	2450	500	39	1.2 µf.
T_{14}	300 "	1000	300	36	.5 µf.
T_{15}	60 "	3000	-	39	2.5 µf.
T_{16}	60 "	2400	500	39	3 µf.
T_{17}	180 "	1300	-	36	.7 µf.
T_{18}	180 "	1000	300	36	1.5 µf.
T_{19}	60 "	2400	500	39	3 µf.





ALL RESISTORS 1/2 W UNLESS OTHERWISE SPECIFIED.
ALL BY-PASS CAPACITORS 25µf 25V

FIG. 5
CIRCUIT DIAGRAM OF THE DIVIDER CHAIN OF FIG. 4

coupling capacitors were chosen following the objective mentioned in the description of the preceding divider stage. Connections are made to the output stages consisting of a type-12AT7 double triode, which supplies a 2-milliwatt 100 cycles/second signal to a 500-ohm output load and 300 cycles/second carrier voltage for the ring modulator input of the fourth divider. As in the first and second divider stages, the tuned transformers T_{13} and T_{14} provide additional frequency discrimination and match the low impedance loads to the plate resistance of the output stages.

The fourth divider stage generates one-fifth of its input frequency of 300 cycles/second which is applied to the input of the ring modulator M4. The 60 cycles/second output component of the ring modulator M4 is amplified in the type-12AT7 triode, which is tuned to this frequency by means of the resonant circuit T_{15} and T_{16}. The output of this triode is connected to the signal input of the second ring modulator M5. The 180 cycles/second output of the ring modulator M4 is amplified in the second type-12AT7 triode which is tuned to this frequency by means of the resonant circuits T_{17} and T_{18} and is applied to the carrier input of the ring modulator M5. The output of this ring modulator, containing frequency components of 120 cycles/second and 240 cycles/second, is connected to the signal input of M4. The potentiometer in the grid circuit of the 60 cycles/second stage is used for gain control. The gain should be adjusted so that the ratio of the carrier voltage to the signal voltage of the ring modulator M5 is larger than three-to-one. A tuned output stage, consisting of one section of a type-12AT7 triode matches the 60 cycles/second output to the 500-ohm load.

Conventional components are used for resistors and potentiometers and for cathode by-pass capacitors. The resonant circuits employ mica capacitors for values smaller than 10,000 $\mu\mu$f and plastic moulded paper capacitors for values larger than 10,000 $\mu\mu$f. Initially metallized paper capacitors were used for interstage coupling, but these proved to be unreliable, and have been replaced by the plastic moulded type. All coils employ Ferroxcube pot cores.

The system is designed for 180-volt plate supply and 12.6-volt filament supply, but it has been found that the first three divider stages operate satisfactorily with 110 volts on the plate. Since longer tube life can be expected with lower plate voltage, a voltage dropping resistor and by-pass capacitor have been provided to supply these stages at the reduced voltage.

PERFORMANCE OF THE SYSTEM DESIGN EMPLOYED

The four divider stages described above exhibit similar starting properties. It was found that the circuits are self-starting when there is sufficient gain in the feedback loop or when the input voltage is large. As the gain in the loop or the input voltage is reduced, there is a range where the circuit can be started simply by shorting to ground one terminal of the ring modulator, thus momentarily introducing useful frequency components into the loop. For this purpose four switches, S_1, S_2, S_3 and S_4, are

provided, each for the corresponding divider stage, by means of which starting of operation can be accomplished manually. As the gain in the loop or the input voltage is further reduced, starting is impossible. A slight unbalance of the ring modulator improves the starting ability of the circuit. Output voltage indicators consisting of a microammeter, 12 kilo-ohm series resistor, and a germanium diode (Sylvania 1N39) are connected across the loads of the output stages of all dividers, facilitating maintenance and trouble spotting of the system.

The overall performance of the system was tested with regard to stability of the division ratio, applying variations in the input, plate, and filament voltage and the input frequency. The operating conditions were: plate voltage, 200 volts; filament voltage, 12 volts; input voltage, 2 volts; input frequency 100 kilocycles/second. While one of these parameters was varied, the others were left unchanged. The measured relationship between the output voltage at 60 cycles/second and the input voltage at 100 kilocycles /second, the plate voltage, the filament voltage, and the input frequency, for which the correct overall division ratio is maintained, is shown in Fig. 6 on the graphs "a", "b", "c", and "d", respectively. It is seen that outside the operating range the output

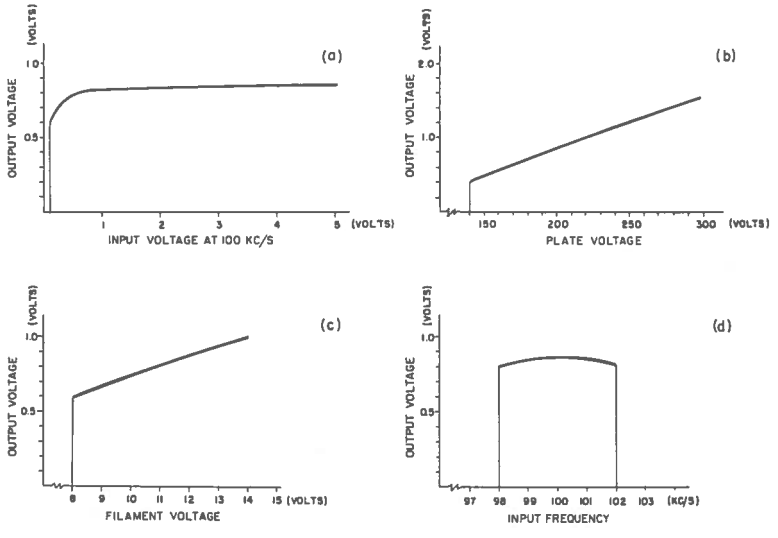


FIG. 6 RESULTS OF MEASUREMENTS ON DIVIDER CHAIN OF FIG. 5 SHOWING RELATIONSHIP BETWEEN OUTPUT VOLTAGE AND (a) INPUT VOLTAGE, (b) PLATE VOLTAGE, (c) FILAMENT VOLTAGE, AND (d) INPUT FREQUENCY

voltage drops sharply to zero. In actual operation the input and the supply voltages are not likely to vary greatly, and the input frequency is practically constant. The

results shown in the graphs indicate then, that satisfactory operation should be expected even though the vacuum tube characteristics or the values of circuit components drift by a considerable amount.

Photographs of the chassis appear in Figs. 7, 8, and 9. The starting switches and output voltage indicators are mounted in the front panel door, and the four compartments, each housing one divider stage, are separated from each other by partitions acting as shields.

ACKNOWLEDGEMENT

The author wishes to express appreciation to Mr. J. C. Swail for his interest and helpful suggestions, and to Mr. S. Keays for his eager and able assistance during the development and maintenance of this divider chain. Mr. E. J. Doyle wired and aligned the chassis and carried out the measurements shown in the graphs of Fig. 6.

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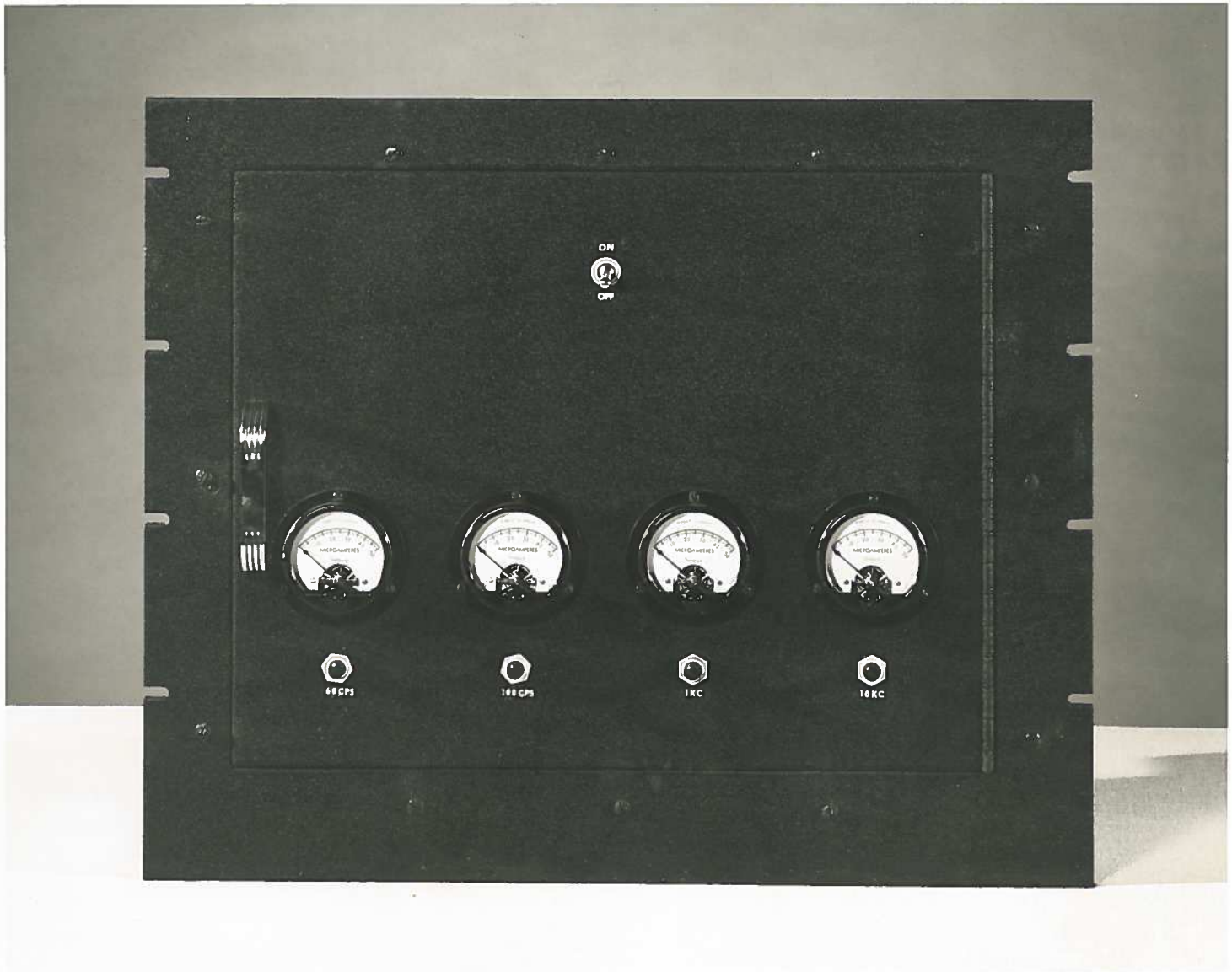

FIG. 7 CHASSIS OF DIVIDER CHAIN OF FIG. 5
Front View

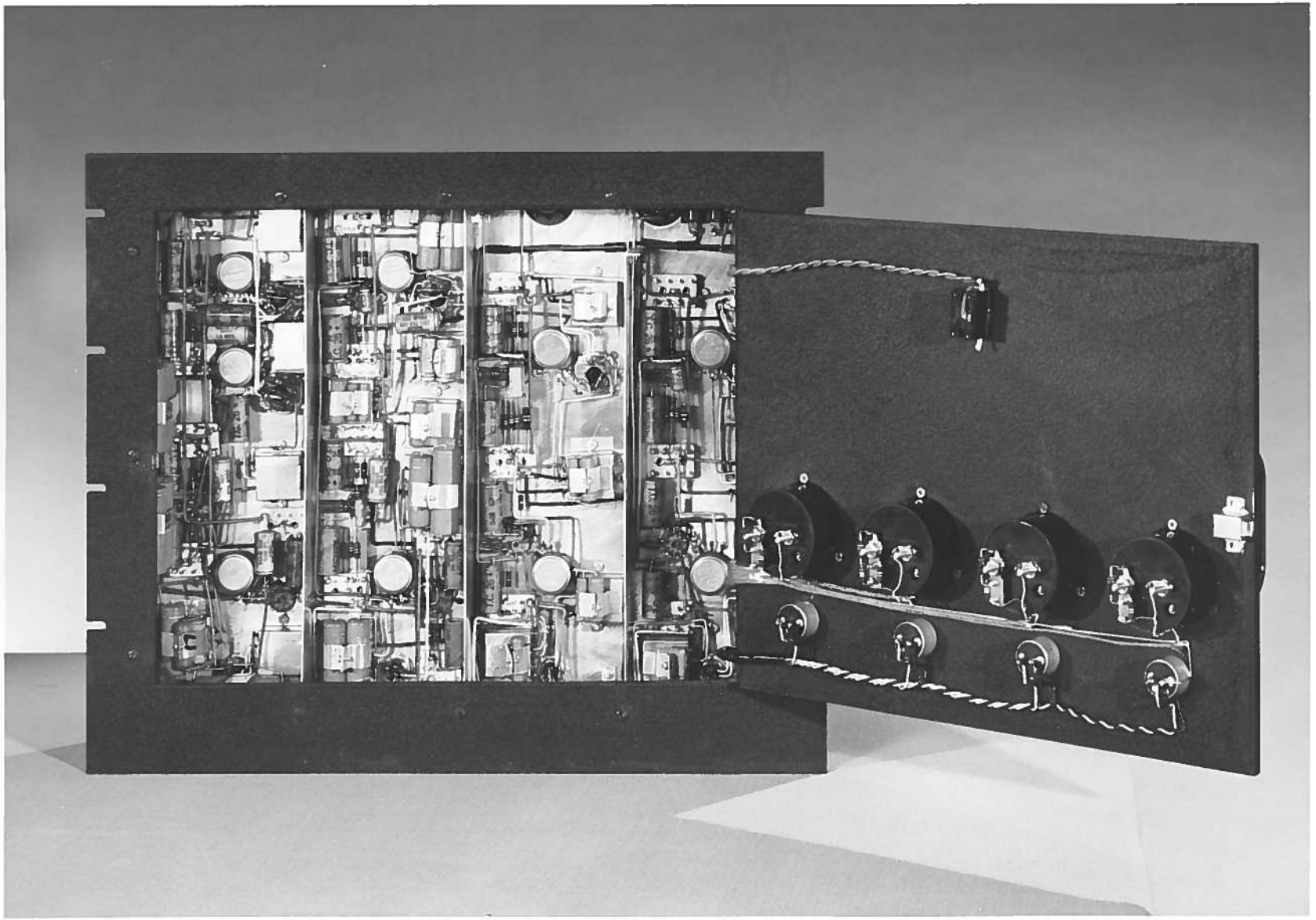

FIG. 8 CHASSIS OF DIVIDER CHAIN OF FIG. 5
Front View with Front Panel Door Open

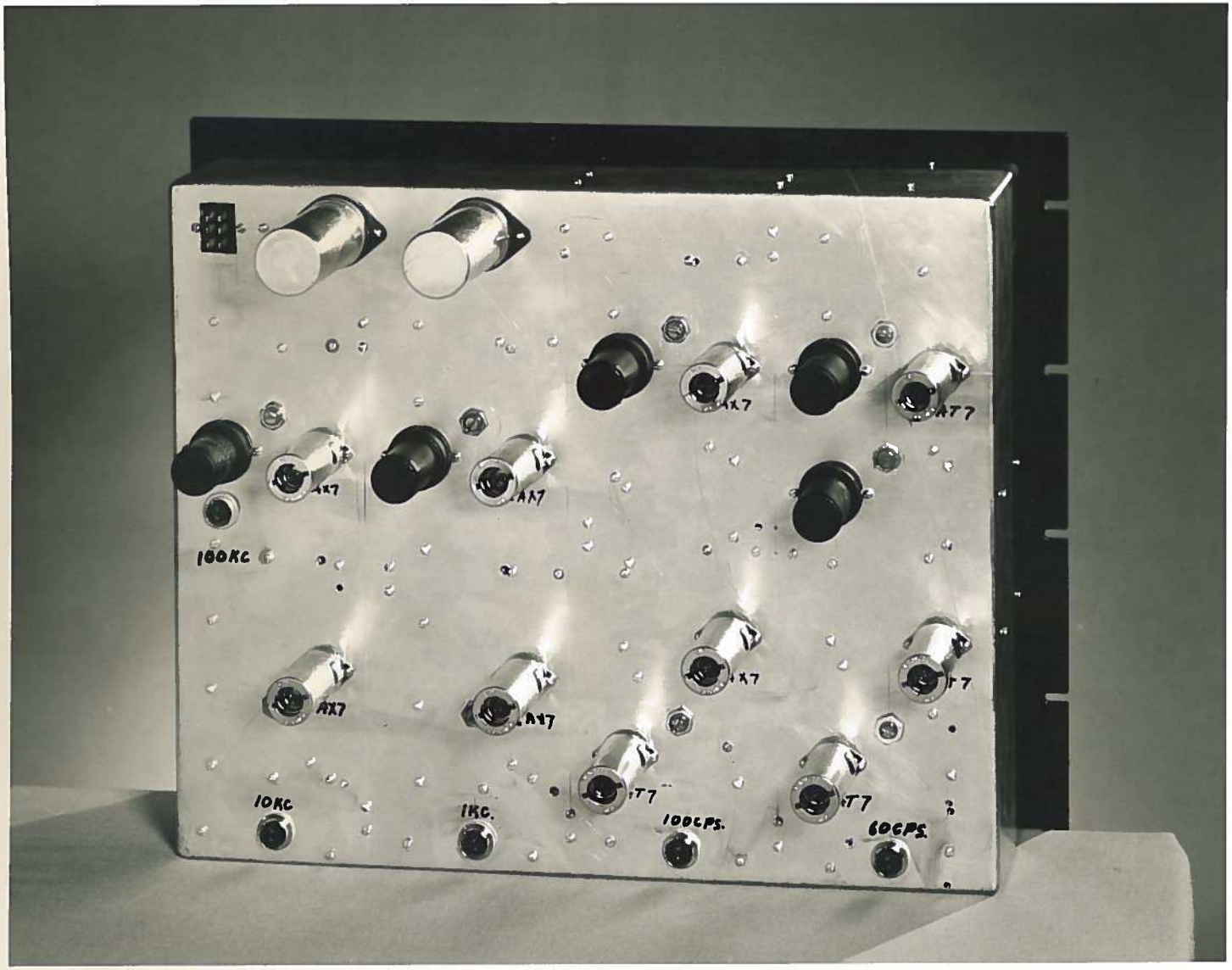

FIG. 9 CHASSIS OF DIVIDER CHAIN OF FIG. 5
Rear View