Hardware reference manual for digital CRT display

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HARDWARE REFERENCE MANUAL FOR DIGITAL CRT DISPLAY

– G.H. Bechthold –

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ABSTRACT

A display processor used to interface a 21-inch cathode-ray tube display with a small research computer is described. Inputs from an external 4K memory, incremental and absolute shaft position encoders, and data/control switches are also provided. In addition to the point-plotting and single-character mode of the display, a line generator using incremental binary rate multiplier techniques is incorporated for drawing vectors, circles, and parabolas. A character sequencer allows 4 characters per 24-bit word to be displayed, and also provides automatic carriage return and line feed for text displayed on the CRT screen.

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HARDWARE REFERENCE MANUAL FOR DIGITAL CRT DISPLAY

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INTRODUCTION

A display processor for use with a modified 21-inch CRT display* with the SEL 840A† computer, and with other peripheral equipment has been constructed to study hardware [1] and software [2] for use in man–machine communications. Changes to both hardware and software are being made continuously as new ideas are tried and old ones are modified. Therefore, the information contained in this hardware reference manual applies to the equipment as of September 1968.

To facilitate changes, the hardware has been constructed of DEC§ plug-in, modular, logic boards. Information for the interconnection and operation of these modules is contained in Ref. 3. This handbook also describes typical logic configurations for up/down counters similar to the types used for position and rate counters in the display processor.

The display consists of a 21-inch CRT, x and y magnetic deflection circuitry, a character generator which drives electrostatic deflection circuits, and the associated power supplies.

GENERAL DESCRIPTION

Control and Data Flow

The display processor has been developed to control a 21-inch CRT display and to interface it with several data input sources. The processor circuits permit the various data sources to control the display of points and characters and to generate scaled vectors, circles, parabolas, 4-character groups, analogue outputs, and interrupts to the 840A computer. These data sources (shown in Fig. 1) are: 840A computer, an external core memory of 4K 26-bit words, absolute shaft position encoders, incremental shaft position encoders (MOUSE), operator control switches, and an internal event counter and position (x, y, and SIGN) registers. Under control of the command register, these inputs are loaded into a data register (D. REG.) from which they can be distributed to the following: x or y or x and y position registers, Δx and Δy rate and sign registers, character register, intensity register, scale register, event counter, 840A processor, and a digital-to-analogue (D/A) converter (not shown in Fig. 1).

The command register (C. REG.) shown in both the simplified block diagram, Fig. 2, and in the more detailed diagram, Fig. 3, is used to control gating and timing of the circuits in the display processor. It may be loaded with command words from the 840A or the external memory. The control switches can also be used, for test purposes, to load the C. REG.

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* Information Devices Incorporated
† Systems Engineering Laboratories
§ Digital Equipment Corporation

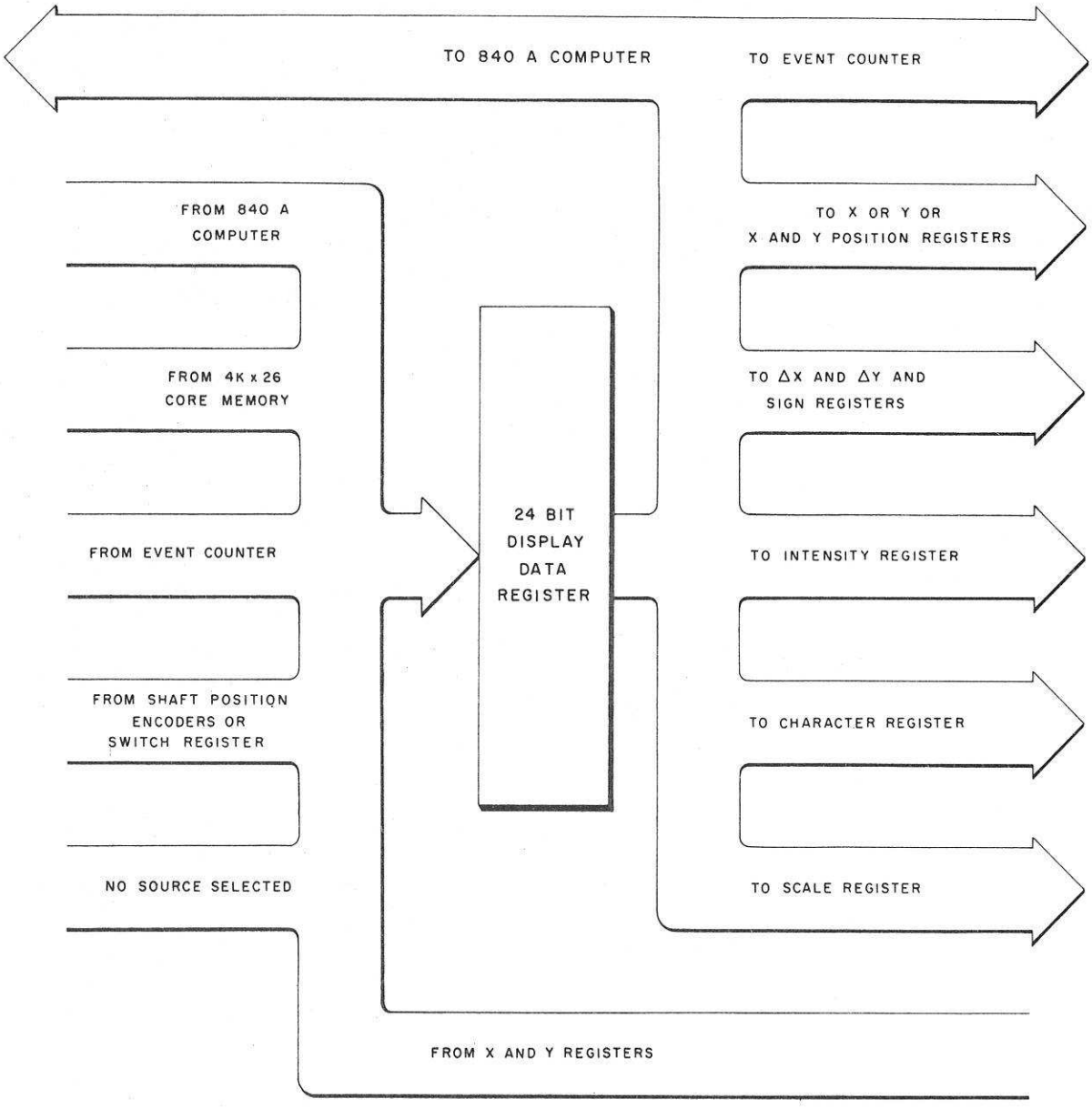


Figure 1 Block diagram of the display processor data routing

The two units which control the display processor (840A and external memory) transmit commands and data over their respective 24 input lines. The corresponding command or data strobe, which is transmitted over a separate control line when the information is present, loads the C. or D. REG. and thus separates commands from data.

One of the two extra bits of the external memory 26-bit word is used to flag command words so that the proper strobe may be issued with the word being read out. This command flag bit is set, during loading from the 840A, by a command external unit (CEU) strobe.

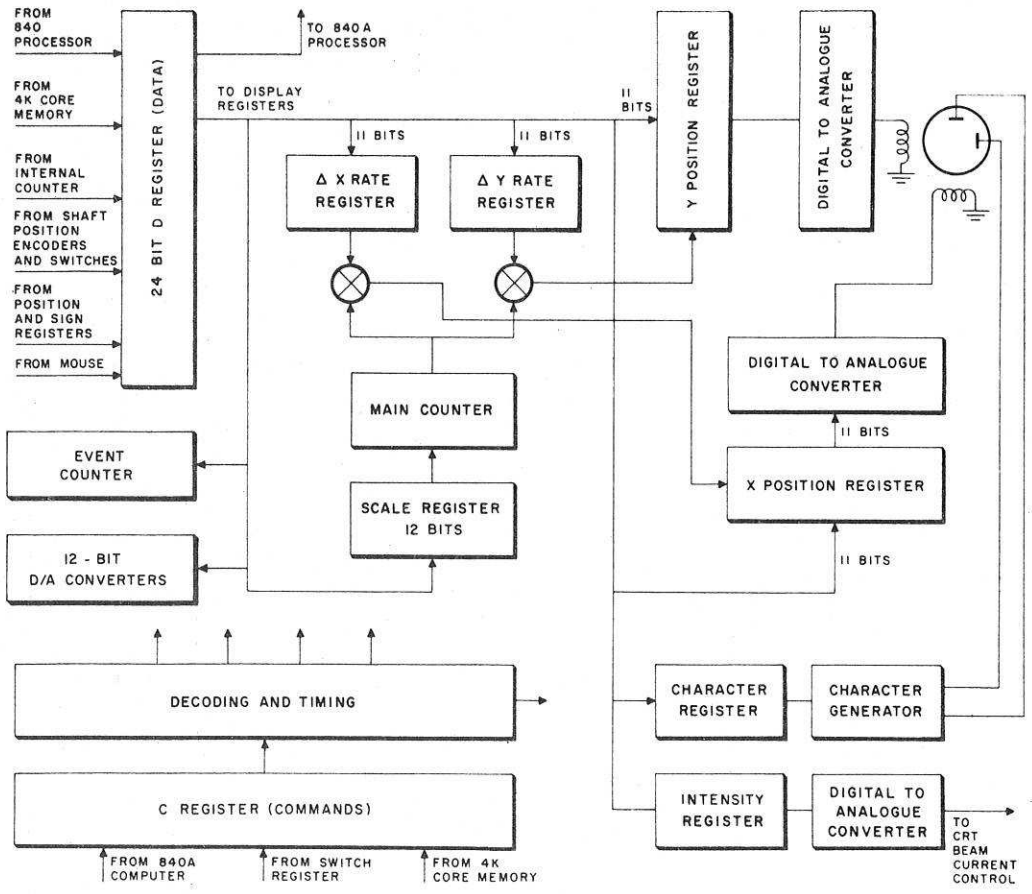


Figure 2 Simplified display control electronics

When transferring data between the 840A and the external memory under block transfer control (BTC) only 24-bit words are transferred and the flag bit cannot be set. To allow the display to operate from the external memory, which was loaded under BTC, an all-zero word is used to indicate that the next word is a command. A circuit in the display processor detects this all-zero word and generates a command strobe for the word following.

Point-Plotting Mode

Before a point is displayed, its position is loaded into the x and y registers and the required intensity is loaded into the intensity register. The CRT beam is then positioned by the electromagnetic deflection circuits which are driven from the x and y registers via D/A converters.

Owing to the slow response time of the magnetic deflection circuits when widely separated points are plotted, time must be allowed for the CRT beam to settle. For this reason the point strobe, which gates the intensity circuits within the display, is

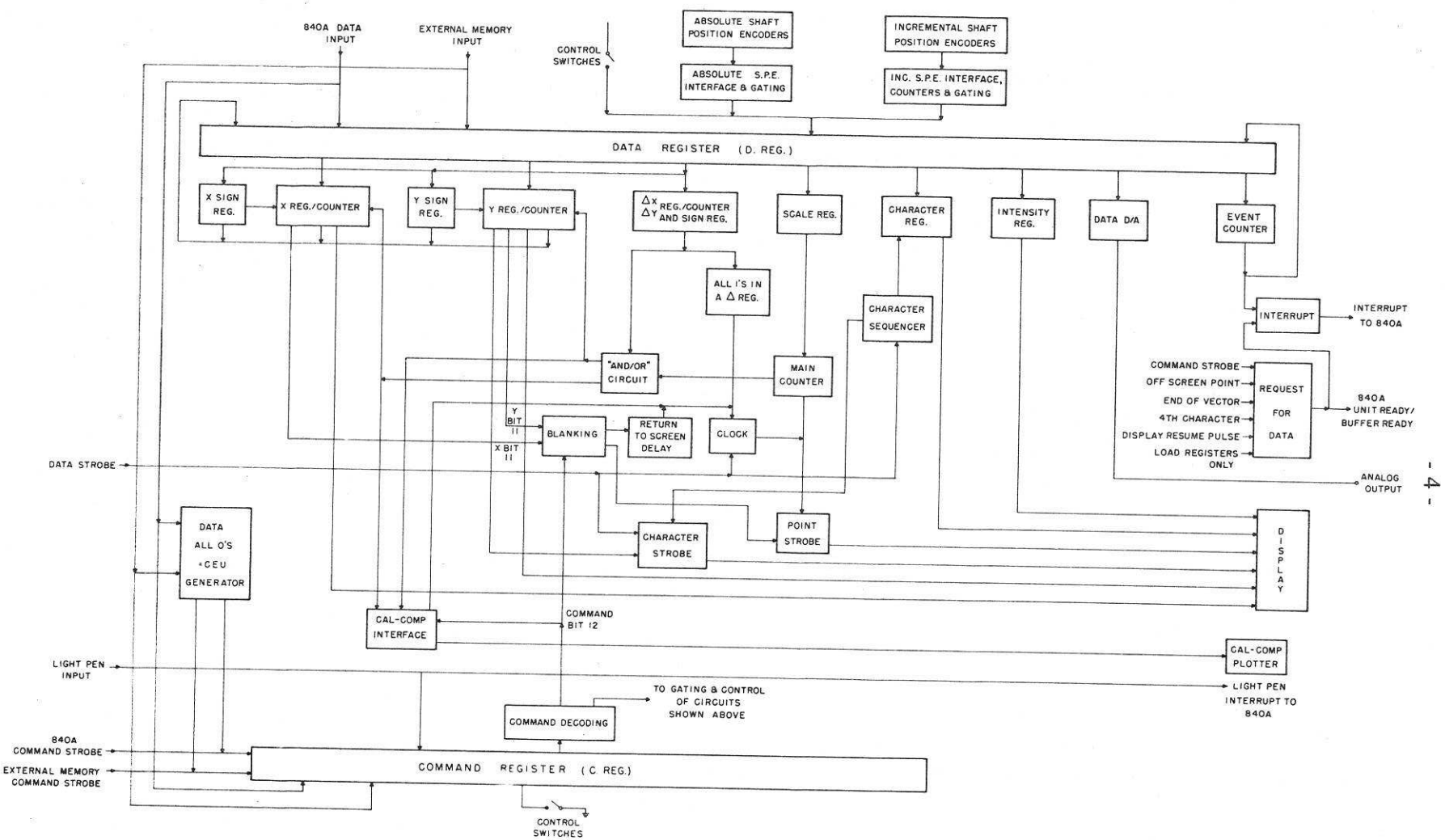


Fig. 3 Block diagram of display electronics

generated ≈ 70 μs after the D/A converters are loaded. For closely spaced points the beam settling time is less. Command bit 13 can, for such points, be set to reduce the strobe delay to ≈ 15 μs, thus decreasing point plotting time and CRT flicker.

Character-Plotting Mode

Three modes of character plotting are available: single-character, 4-character, and x-position with a single character.

In the *single-character* mode the bits 0 to 5 are transferred from the D. REG. to the character register and a character strobe is sent to the display to trigger its character generating circuits. In response to the binary signals from the character register, the stroke-type character generator in the display provides the appropriate analogue signals for intensity gating and for driving the electrostatic deflection circuits. Although the electrostatic deflection circuits have a higher writing rate than the electromagnetic circuits, they are limited to small deflections and are used only for the display of characters. The characters are positioned by the electromagnetic deflection circuits as described for point plotting.

Four characters of 6 bits each may be displayed consecutively from a single data word. A character sequencer gates these 6-bit binary groups, beginning with the 6 most significant bits, from the D. REG. to the character register when operating in the *4-character* mode. It also increments the x register after each character is plotted and decrements the y register (line feed – L.F.) when the x register changes from all *ones* to all *zeros* at the end of a line of text (carriage return – C.R.). At the end of a line, a 100-μs delay is enabled to delay the first character strobe after a C.R. This time allows the CRT beam to fly back and settle before beginning the first character of the next line.

The *x-position and single-character* mode of operation is similar to that of the single-character mode but the character sequencer is forced to its fourth position thus loading bits 18 to 23 of the D. REG. into the character register.

Vector Mode

The x and y registers are capable of being operated as up/down counters with their associated binary rate multipliers (BRM) [4]. As the value in the register changes, the spot on the screen moves and can be made to generate vectors, $\frac{1}{4}$-circle arcs, or parabolas. The operation of the BRM begins when the main counter is loaded with a number contained in the scale register. The vector clock is then started and this causes the main counter to effectively count down to zero and stop the clock. Pulses generated by the transitions in the main counter are gated by lines coming from the Δx and Δy registers in such a way as to produce pulse trains going to the position registers at rates proportional to Δx and Δy, respectively. The result is to plot a vector on the screen with components equal to Δx and Δy, respectively [1], and a length proportional to the value

loaded into the main counter from the scale register. If the Δx and Δy registers are allowed to count, then curved lines are produced [1, 4].

To generate lines with parabolic curvature, the value in the Δx or Δy rate registers is made to vary with time by having them incremented with pulses from the (vector) clock.

Circles are composed of four $\frac{1}{4}$-circle arcs generated by the display processor and displayed in sequence. These $\frac{1}{4}$ circles are generated by setting one rate register as an up counter with zero value and the other as a down counter with an initial value proportional to the radius of curvature. The BRM's are cross coupled so the output of the Δx multiplier decrements the Δy rate register while the Δy multiplier increments the Δx rate register. This cross coupling results in the output rate of one BRM being the integral of the other BRM and vice versa, thus producing sine and cosine values in the position registers.

The completion of the $\frac{1}{4}$ circle arc is indicated by the all-zero state of the rate multiplier which contained the initial value for the radius of curvature. A circuit to stop the vector clock when an all zero condition in the BRM's is reached could prevent the clock from operating, as one of the rate multipliers is initially in an all-zeros condition. By using a circuit which detects the all-ones state, the next state occurring after the all-zeros state, the initial condition problem is overcome and the additional pulse to the position registers is negligible for practical purposes.

When the position registers are incremented and the CRT spot leaves the edge of the screen it would normally appear on the opposite side of the screen as the D/A converters are connected to the 10 least significant bits (LSB) of the position registers and these repeat after the spot reaches the edge. To prevent this, the eleventh bit of the position registers blanks the beam until the position registers are decremented and the vector returns 'on screen' or the position counters are cleared. However, the blanked beam must cross the entire screen between adjacent points when returning on screen, so a delay is introduced for the first on-screen point by stopping the vector clock to allow time for the point to settle before intensifying.

Cal-Comp Plotter

The Cal-Comp incremental plotter is advanced by the same Δx and Δy BRM pulses which advance the x and y counters when drawing vectors. The pulse rate is limited to the maximum input rate for the plotter of 300 pps. A fairly constant pulse rate near this maximum is obtained when drawing vectors on the plotter by stopping the vector clock, which operates at greater than 0.5 MHz, for approximately 3.5 msec when there is an output from either BRM. This allows time for the plotter to respond to a pulse before receiving the next. If the clock were slowed down until the maximum rate of the BRM was within the capabilities of the plotter, the pulse rate would vary considerably for various vectors depending upon their slope. Thus the plotter will draw vectors but it lacks the absolute positioning required to reproduce points and the speed to be able to plot characters provided by the character generator.

Event Counter

The event counter may be used to count or to raise an interrupt after being decremented to zero from a preset value. The counter is loaded from the D. REG. and may also be transferred to the 840A for readout.

Request for Data

The REQUEST-FOR-DATA circuit signals the 840A or external memory, with which the display processor has been operating, when the operation in progress has been completed. This allows the controlling unit to initiate the next operation. When operating in the memory mode and a REQUEST-FOR-DATA is raised, a UNIT READY/ BUFFER READY signal is sent to the 840A for 1.2 μsec. If the computer is waiting to use the display, it can take over operation of the display by changing the command register. If the external memory was using the display and the 840A did not steal control during the 1.2 μsec, the REQUEST-FOR-DATA to the external memory will be issued 5 μsec after the request to the 840A was initiated. The 3.8-μsec time gap from the removal of the UNIT READY/BUFFER READY signal until the request is made to memory is to allow time for the computer to issue commands it began during the 1.2 μsec UNIT READY/BUFFER READY signal. When the display processor is not in the memory mode, a UNIT READY/BUFFER READY signal remains until cleared by the next data or command strobe received from the 840A. The REQUEST-FOR-DATA signal can also raise an interrupt to the computer if that interrupt has been enabled by a command to the C. REG.

DETAILED CIRCUIT DESCRIPTION

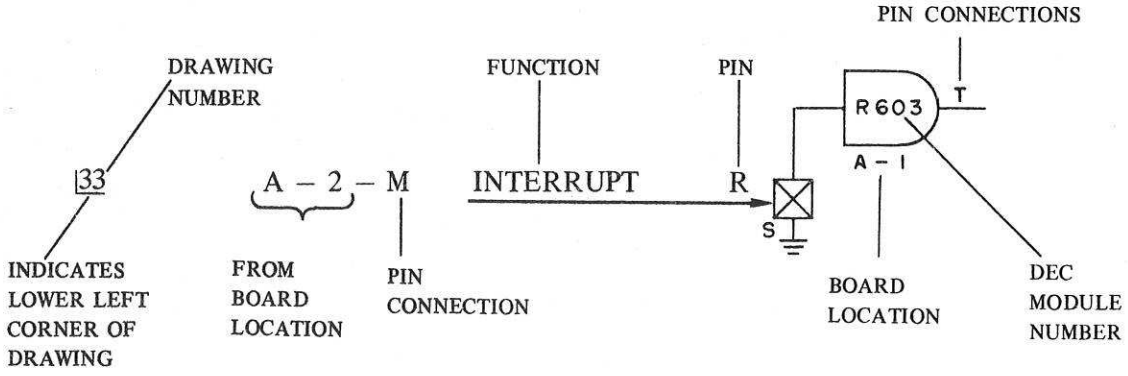
Circuit Board Functions and Locations DS-1-14D

The information on drawing DS-1-14D is shown as viewed from the wiring side of the circuit board connectors. The circuit board function drawing contains numbers in brackets which refer to the drawing number for that particular circuit. The circuit boards listed on the location drawing are DEC flip chip modules with the exception of the following NRC assembled boards: DSO-12A, I.C.G., S.P.E. INV., x and y D/A, ±15-V P.S. and +5-V P.S. Information related to the flip chip boards can be obtained from the 'Digital Logic Handbook, Flip Chip Modules', by Digital Equipment Corporation.

Description of Symbols and Labels Used

The 24-bit command words are usually described by giving an octal number for one of the eight 3-bit groups X, B, C, ... H (e.g., '7 group H). When one individual bit is referred to, it may be identified by its bit number (e.g., bit 8). Bit numbers of the data register are shown in a triangle and those of the command register are surrounded by a circle. The DEC flip chip module numbers are shown within their symbol and the letter-numeral combination under the symbol indicates the circuit board location.

Connections coming from or going to another drawing are illustrated by the following example:



The flip flops are enabled by a zero and triggered by a -3-V to 0-V transition.

Format

The display command format (Fig. 4) is also shown in more detail on drawing DS-1-13D. The command word is broken up into 8 octal groups. The B, D, G, and H groups are decoded by binary-to-octal converters while the bits of the C, E, and F groups are used as individual bits. The bits of the 1st octal group (x) are not used. The H octal group indicates the source from which the D. REG. is loaded. The G group identifies the destination to which this data will be transferred.

Shown with the data formats are the associated command words for loading the appropriate register.

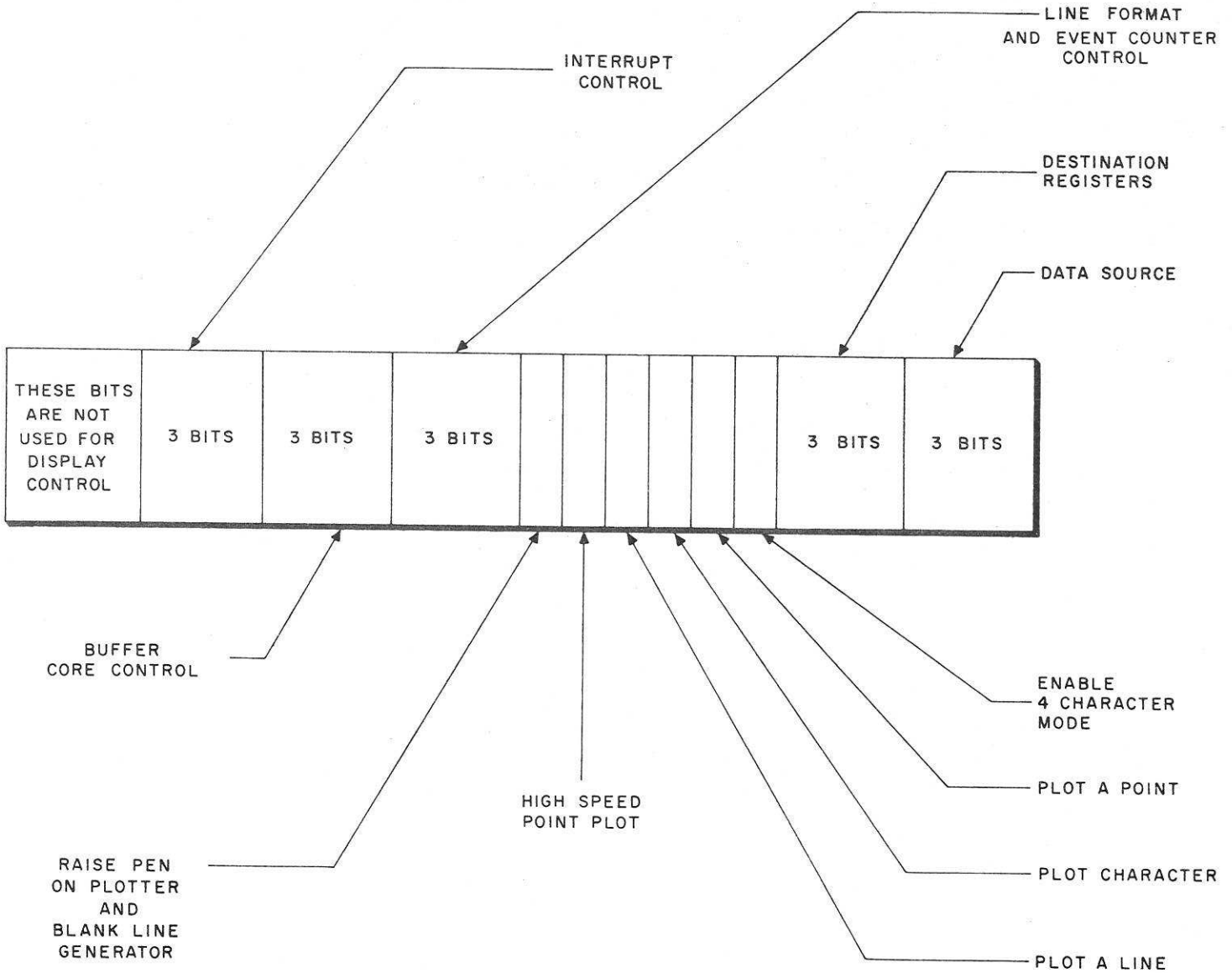


Figure 4 Display command word format

Command Register DS-1-15D

The command strobes from the 840A or the external memory are OR'ed by the A-1 pulse generator which clears the C. REG. with the exception of bit 8. These command strobes are delayed approximately 0.5 μsec by A-2 before a load strobe is issued to the appropriate diode-capacitor-diode (DCD) inputs. This allows set-up time for the flip flop DCD gates. The delay is achieved by using an R203 flip flop with an external network connected from the output to the direct-clear input to reset the flip flop after the appropriate delay. Inputs to the C. REG. are the outputs of the 840A and external memory level changers shown on DS-1-17D.

Bit 8 of the C. REG. is jam transferred from the 840A level changer only, but it may also be cleared by an interrupt, a manual clear, or by an enabled light pen input. The flip flop (Y-17), which enables the light pen to clear bit 8, is set by a '4 group B of the C. REG. and is reset when bit 8 is cleared.

Clear-Load Circuits DS-1-16D

The clear-load circuits on drawing DS-1-16D gate the required clear and load strobes for all the display registers with the exception of the command register and the event counter. The three data strobe sources, which begin the clear-load operations, are: *a*) the combined 840A or external memory strobe, *b*) the operator control switches, or *c*) a delayed command strobe. This delayed command strobe is gated to the data strobe input for the five data sources which do not generate their own data strobes. The 840A and the external memory are the only units which provide their own data strobes. Either of these two may issue a command to input from one of the five sources. After a 1.2 μsec delay, provided by ⌊15 A-2-T, a data strobe is issued to input the data presented to the D. REG. by this source. The REQUEST-FOR-DATA to the controlling source, which would normally occur after the command strobe, is inhibited until the data have been transferred to the register specified in the command. The next word is then requested in the normal manner by a REQUEST-FOR-DATA.

The data register must be cleared before loading from inputs specified by '0 to '3 group H and set before loading from the complement of '4 to '7 group H inputs. The most significant bit of group H (bit 21) performs this gating directly at ⌈16 B-6 with no extra decoding required. After approximately 0.5 μsec, the D. REG. is loaded by $\overline{16}$⌋ B-7 or B-8 as determined by the H group of the C. REG. At this time, the register designated by the G group of the C. REG. is also cleared and after a 0.75 μsec delay by $\overline{16}$⌋ B-5-M, it is loaded. When the selected register has been loaded, $\overline{16}$⌋ B-5-T provides a further delay before generating the delayed data strobe which is used to begin the plotting of vectors, points, or characters, or to initiate a REQUEST-FOR-DATA if none of these plotting modes has been selected.

The ALL 0 DATA = CEU circuit is shown in the lower left corner of drawing DS-1-16D. The condition where an external memory data word is all 0 and the display is operating from the external memory will be illustrated. An all 0 condition at the output of the external memory level changer is detected by ⌊16 Y-21 and Y-22, and is ANDed with an inverted data strobe and the complement of C. REG. bit 8. This condition sets flip flop ⌊16 Y-19-T which enables ⌊16 Y-19-E and disables ⌈16 B-7-S. After the delay by ⌈16 B-5-F, the data strobe sets ⌊16 Y-19-D but is prevented from generating the register clear and D. REG. load by the disabled ⌈16 B-7-S. When flip flop ⌊16 Y-19-D is set, its output is ANDed with the complement of bit 8 and the inverted clear D. REG. pulse. The D. REG. clear pulse occurred before the load D. REG. pulse used to set ⌊16 Y-19-D, so there will be no output from the AND circuit until the next data strobe arrives. This second data strobe will be gated through and be ORed into the command strobe input ⌊15 B-2-J, thus loading the data word following an all 0's condition into the C. REG. When the C. REG. has been loaded a delayed command strobe is issued which clears both ⌊16 Y-19 flip flops. This clearing initiates a REQUEST-FOR-DATA from circuit ⌊16 B-3-M.

When the display processor is not in the external memory mode, a similar group of gates look for the above conditions from the 840A.

Data Register DS-1-17D

The D. REG. can be loaded from seven sources under control of group H of the C. REG. For sources '0 to '3 the register is cleared. It may then be loaded, through its set inputs, for sources '1, '2, or '3. The D. REG. is not loaded for '0 and it remains in the 0 (cleared) state. For input sources '4 to '7 the D. REG. flip flops are set so that their clear inputs may be loaded with the complement of signals '4 to '7. Inputs '5, '6, and '7-H are OR'ed and applied to one input of the flip flop.

The drawing illustrates only one stage or bit of the D. REG., the others being the same with the input sources listed in the table below. The bit number is given in the left column, the location of the flip flop for that bit is next, and under the appropriate flip flop inputs, the data sources are listed including the level changers used with the external memory and the 840A. The appropriate clear and load strobes come from the circuits shown on drawing DS-1-16D.

Event Counter DS-1-37D

When the event counter has been cleared, it may be loaded with the complement of the D. REG. so it will reach an all 1's state after being incremented the number of times originally loaded. On the next increment the counter will advance to zero and raise an interrupt.

If the counter is first cleared, then incremented a number of times, this number may be transferred from the event counter to the D. REG. and thus be made available to the 840A. The complement output of the event counter is used for this transfer as the data are entered through the complement side of the D. REG.

Control Switch Panel DS-1-19D

The control switches are provided for manually entering commands or data and may be used to operate the display for simple checking procedures. The center-off control switches ground the C. REG. outputs when operated in the down (momentary) position and force the selected bits on. The command-clear switch operates a pulse generator to produce either a single clear pulse (switch down) or a train of clear pulses (switch up) that are generated by a free running clock R401.

When the control switches are in the up position, they connect to a D. REG. input. If the switches have been enabled by '7 group H of the C. REG., those set will load 0's in the D. REG. when it is strobed. In their normal center-off position the D. REG. will be set to 1's when it is strobed.

To load the D. REG. manually from the switches, a '7 group H is first entered in the C. REG. by depressing the appropriate switches. The switches which represent 0 data bits are then raised and a data strobe is generated by use of the data strobe switch. In the up position this switch gates the free running clock R401 to a pulse generator to produce repetitive strobes and in the down (momentary) position generates a single strobe. The repetitive mode is useful for displaying the information entered in the D. REG. for test purposes.

The lamp drivers W050 and their associated lamps connect to the complement output of the C. REG. to indicate the state of the flip flops and thus the command present in the register.

Absolute Shaft Position Encoders DS-1-18D, DS-1-42D

The circuits used for the two shaft position encoders (SPE) are the same except for the board locations. Only one unit is shown and the board location for the other unit is indicated in brackets.

The encoder shown on the left of the drawing is a commutator unit that provides an absolute readout of shaft position. The outputs, which are either open circuited or at -3 V, are interfaced by the SPE inverters (circuit DS-1-42) with the DEC circuits that require a ground or a -3 V signal. The R111 gates provide the gating required to generate the least significant bit (LSB) from the SPE outputs. The R107 inverters 18| A-12 (A-13) are used to force the outputs of the SPE circuits to -3 V when they are not selected by the C. REG. This allows their outputs to be OR'ed directly with the outputs of the incremental SPE and the control switches.

Incremental Shaft Position Encoders DS-1-38D, DS-1-46D
Up/Down Counter (12 Bit) DS-0-9D

The incremental SPE outputs are amplified and squared by the circuits shown on drawing DS-1-46D and are then sent to the W501 Schmidt trigger boards (drawing DS-1-38D). The W501's standardize the pulses to DEC levels and drive R202 (the up/down flip flop) and the counter. The two pulses coming from the SPE differ in phase by approximately 90°. The R202 flip flop detects which arrives first and is set to the corresponding state. When the direction of the SPE is changed, the order of the pulse arrival changes and thus alters the up/down flip flop. The counter must be disabled while its up/down state is changed. The R204 delays the up/down signal so R602 can first disable the counter. The output of the counter is gated by the R113 gates, then is ORed with the absolute SPE and the control switches.

The 12-bit counter (drawing DS-0-9D) is constructed of RTL circuits with the required gating of flip flop outputs to produce an up/down counter. The circuitry is operated with V_{cc} grounded and the regular ground (emitter) connections supplied with -3.6 V. The inverters are used to provide sufficient drive for the DEC circuits.

Output Level Changers DS-1-39D

The DSO-12A level changers provide the interface necessary to transfer data from the D. REG. to the 840A. One unit is illustrated, with the board locations and connections for the others listed in the table.

Data Register D/A Converter DS-1-34D

This drawing shows one of the inverters used to drive the data register D/A converters, and the table of connections from the D. REG. to the inverters and to the D/A converter.

Main Counter and Scale Register DS-1-25D

The scale register is cleared and loaded with data from the D. REG. by strobes from the circuits shown on the clear-load drawing DS-1-16D.

The main counter is cleared by every data strobe through the $\lceil\overline{16}$ C-12-R inverter. The 10 least significant bits (LSB) are cleared to zero and the 2 most significant bits (MSB) are set to 1. If the counter is not loaded but is incremented by the vector clock it will produce an output to stop the clock one increment after the 10 LSBs have reached 1. This results in a vector called a full scale vector and is capable of generating a full screen corner-to-corner vector. If some of the counter's 10 LSBs are loaded, the vector will be shorter than full scale, and if either or both of the two MSBs are set, the vector will be longer than full scale. These last two flip flops differ from the other stages of the counter. Their input must be complemented because their outputs are taken from the complement output. The MSB flip flop would be triggered when the second MSB is loaded if the diode-capacitor-diode (DCD) gate $\overline{25}\rceil$ F-19-K was not disabled by the cleared $\overline{25}\rceil$ F-24-E. The logical delay of the DCD gate allows it to remain disabled when the counter load pulse arrives.

Δx Counter DS-1-22D

Δy Counter DS-1-23D

The operation of each of these counters is similar to the up/down counter description given in the DEC Logic Handbook [3]. They are, in addition, capable of being cleared and loaded. The sign flip flop in the lower right corner controls the up/down state of the counter and inputs from the vector clock, and the other rate multiplier (Δx or Δy and its associated gates) is applied to the first stage on the left. Use of these inputs is described under the General Description, binary rate multipliers and second order curves [4].

All Ones in a Δ Register DS-1-24D

This AND circuit is used to stop the vector clock when in the circle mode and an all ones condition is detected in one of the rate counters, indicating the completion of a $\frac{1}{4}$ circle arc.

AND/OR **Circuit DS-1-26D**

The (DCD) gates of the R601 perform the ANDing operation with the pulse inputs detecting the positive going edge of the main counter and the level inputs gated by the rate counters. The outputs of the AND circuits are ORed to produce the binary rate multiplier (BRM) output pulses. An additional input of the Δx BRM gate is used to produce pulses which increment the x register every time the y register is loaded. In this way a sweep is generated for the x axis and an oscilloscope type of display may be easily presented.

x Register DS-1-27D

y Register DS-1-28D

These up/down counter-registers [4] are similar to the rate counters and to the up/down counter described in the DEC Logic Handbook [3]. One difference is the pulse generator |27 and $\overline{28}$| E-25 which normally passes the pulse from one stage to the next, thus allowing the counter to operate in the conventional manner. In the 4-character mode of operation the x register is incremented by the RESUME pulse from the display at the fifth stage of the counter. This gives the proper spacing for the letters of the 4-character groups. The x register transition from all ones to zero at the end of a line of text triggers the pulse generator that increments the eighth stage of the y register. This provides the appropriate spacing for the next line of text.

The sign flip flops, which control the up/down state of the counters, can be cleared and loaded from the D. REG. by Δ strobes but are forced to the x positive (right) and y negative (down) state in the 4-character mode. This displays text from left to right, top to bottom of the CRT screen. These flip flops are set to this state by the strobe to the display ANDed with command bit 17 (4-character mode).

When plotting points, the position counters are loaded from the D. REG. and for vectors and curves they are incremented by their appropriate binary rate multiplier. The BRM inputs are disabled by $\overline{16}$| B-5-M when the main counter is loaded to prevent spurious pulses that occur from incrementing the x or y counters.

Display D/A Converters DS-1-31D

One of the two display D/A converters and its associated level changers is shown. The other D/A is similar, with its board locations and connections shown in brackets where they differ. The power supplies are common to both units.

Cal-Comp Drivers DS-1-32D

The circuits on this drawing are used to operate the Cal-Comp plotter which produces $x-y$ vectors on paper. The monostable multivibrators [32] Z-3 and [32] Z-4 are used to produce the required pulse width ($\approx$ 12 μsec) for the plotter which is driven by the W600 level changers. The BRM outputs are ANDed with their respective signs and the delayed data strobe is ANDed with command bit 12 (pen up/down) to trigger these multivibrators except when disabled by gates [32] Y-15. These gates are disabled immediately prior to loading the registers so the plotter will not receive stray pulses from the BRMs when the main counter is loaded. The diodes ([32] Y-3) prevent the monostable multivibrators from operating when the front panel control switch is in the display position. When the switch is in the plotter position, the circuit, which stops the vector clock for approximately 0.3 sec to allow time for the pen to be lowered, is enabled. The flip flop 32| A-4 produces a pulse to trigger delay 32| E-8 on the first PEN DOWN signal following a PEN UP condition.

In order to slow the output of the BRM to a rate within the capabilities of the plotter, a pulse from either the Δx or Δy rate multiplier is used to set flip flop |32 Y-2 which stops the vector clock. This also begins a delay by triggering |32 Y-1-E. After a delay equal to the sum of the two delays (Y-1-M & V), |32 Y-2 is reset. The vector generator continues its operation until the next BRM output when the preceding sequence of events is repeated. Two delays are used in series, each set for approximately half the total delay required, to overcome the problem of dead time after a delay has operated.

Intensity Register DS-1-20D

The intensity register is a two-bit register (data bits 11 and 12) which may be cleared and loaded by the clear and load strobes of the x, the y, or the scale registers. The outputs and their complements are sent to the display through level changers W601.

Character Register DS-1-21D

The 6-bit character register is interfaced by the W601 level changers with the display. It is first set by a strobe $\lceil\overline{16}$ B-7-T, then, if in the 4-character mode, the complement of the signal is loaded into the clear input. When the display has finished plotting this first character, it issues a RESUME pulse which is used to clear the character register. The second character is then loaded from the D. REG. to the set input and is plotted. The third and fourth characters are loaded in a similar manner with the character register being cleared by a RESUME pulse and being loaded on the set input. The strobes for loading the 4 characters are provided by circuitry on the vector-character control drawing, DS-1-29D, while the positioning is controlled by the pulse generators E-25 associated with the x and y registers for this purpose.

When only a single (the first) character is to be displayed, the RESUME pulse is inhibited from clearing the character register and the vector character control does not advance to generate a load strobe for the 2nd character.

When plotting a single character with x positioning, the 4th character must be used, to be compatible with the data format for x position and intensity. After the character register is set by $\lceil\overline{16}$ B-7-T it is cleared by $\lfloor\underline{21}$ E-13-T, which produces a pulse when the load x strobe is ANDed with command bit 15 (plot a character). This clearing allows the 4th character to be loaded by its load strobe from the vector-character circuits.

Vector Character Control DS-1-29D

Operation of the circuits on this drawing will be described for the various modes of operation of the display processor.

For the point plotting mode, command bit 16 gates the delayed data strobe through pulse generator ⌈29 E-23-U. Its output generates a strobe for the display D/A converters and triggers the controllable delay circuit $\overline{29}$| E-24-V which is also enabled by command bit 16. Command bit 13 controls the length of delay so that closely spaced points may be plotted in 15 μsec while others not flagged by bit 13 will require 70 μsec. The delay output, again gated by command bit 16, triggers pulse generator $\overline{29}$| E-22-U and its output is supplied to the off-screen blanking circuits, the REQUEST-FOR-DATA circuits and $\overline{29}$| E-27-K to generate the required pulse for the display strobe. The level changer for this point strobe ($\overline{29}$| E-32) also provides the gating to inhibit the point strobe for the off-screen condition or for command bit 12 blanking.

In the vector mode the outputs of the BRM's are used to trigger flip flop ⌈29 E-7. Its output is gated with command bit 14 to produce an output from pulse generator ⌈29 E-22-U which generates a strobe as previously described for point plotting. The output of flip-flop ⌈29 E-7 also triggers delay ⌈29 E-24-M which allows the position registers to stabilize before the display D/A is loaded from them. This delay is adjusted in conjunction with the vector clock (CRT mode) to minimize plotting errors when drawing vectors at the highest writing rates. The output of the delay triggers ⌈29 E-23-U to load the display D/A converters.

When operating in the single character mode the delayed data strobe is ANDed with command bit 15 to produce an output pulse from pulse generator ⌈29 E-23-K. This pulse is used to generate a display character strobe via controllable delay $\overline{29}$| F-27-M and pulse converter $\overline{29}$| E-27-U, to AND with the output of gate ⌊29 E-10-F and produce a strobe from ⌊29 E-13-F to load the first character, to set the position register signs for the 4-character mode, and to load the display D/A converters from the position registers through ⌈29 E-23-U.

The two flip flops ⌊29 E-9 form a modulo 4 counter for the 4-character mode. After being cleared by a signal from the clear bus the four states of the counter are decoded in sequence by gates ⌊29 E-10-F, -K, -N, -S. These gates enable the corresponding pulse generators which load the character register when they are strobed. The first character strobe to the display and to load the character register is provided by the delayed data strobe as previously described for single characters. When this character has been plotted, the display issues a RESUME pulse which increments the character counter ⌊29 E-9 and initials delay ⌊29 E-8-F. After a delay of 1.5 μsec ⌊29 E-8-F triggers pulse generator ⌈29 E-23-E and the operations described above continue until the counter reaches the fourth state. When the fourth state is reached the counter and the 1.5 μsec delay are disabled by OR gate ⌊29 E-10-V, which also disables these two circuits when not in the 4-character mode (command bit $\overline{17}$). The delay was triggered when the

counter advanced to the fourth state and will complete the delay pulse after its input has been disabled. Its output will again trigger |29 E-23-K to load and plot the fourth character but the resulting RESUME pulse is inhibited from triggering the 4-character counter or the 1.5 μsec delay. It will be used instead by the REQUEST-FOR-DATA circuit which ANDs it with the output of |29 E-10-S to produce the next REQUEST-FOR-DATA. As described for x and y registers the request for data also increments the x counter to display the 4 characters. When the CRT beam reaches the right edge of the screen (all ones) and the x counter is incremented again to all zeros, returning it to the left edge, it decrements the y counter to position the following line of text.

This triggers flip flop 29| F-25 and increases the delay of |29 F-27 from 7.5 μsec to 100 μsec, thus delaying the next character strobe and allowing time for the CRT beam to settle after flyback. After this delay the character strobe is issued and the flip flop is reset to the short delay.

In the plot x position and single character mode the operation is similar to that described for a single character. The only difference occurs in the character counter which is forced to the fourth character state, after being cleared, by the load x strobe ANDed with command bit 15 (a plot character mode).

Command bit 15 and its complement are transferred to the display character generator by level changers 29| F-28.

Off-Screen Blanking DS-1-30D

The x and y position registers contain an eleventh stage which indicates an off-screen condition but is not used for CRT beam positioning. When the counter is incremented beyond full screen (10 bits) this eleventh bit is set and blanks the CRT beam. The exception to this blanking is for 4 character groups of text. The 10 bits of x register are incremented to a maximum, which increments the y register; then the x register begins again on the left of the page. This second line of text would be blanked if the eleventh bit was set after x was incremented to its maximum, and every second frame of text would be blanked if the y eleventh bit was set when y was decremented beyond the bottom of the screen. To prevent this, |30 D-16-D, -H inhibit the loading of their respective eleventh bits in the 4-character mode (command bit 17) for x as an up counter (positive) and y as a down counter (negative).

The outputs of these eleventh bits are ORed and set flip flop |30 E-11-F, which blanks the CRT beam by inhibiting the CRT point strobe. When the position counters are incremented back on screen, gate |30 D-16-L sets flip flop |30 E-11-T to indicate this condition. At this time, the first point, after returning on screen, would normally be plotted, the display D/A converters loaded, and flip flop |30 E-11-T reset by a point strobe. The point is not plotted, however, because the point strobe to the display is still inhibited by the off-screen blanking flip flop |30 E-11-F. The resetting of flip flop |30 E-11-T initiates a delay, |30 E-11-M, which stops the vector clock for 170 μsec. This is to allow time for the transients in the deflection circuits, caused by full screen deflection between adjacent points, to settle before continuing the vector. After this delay, the vector clock is allowed to continue and the delay |30 E-11-M resets the blanking flip flop |30 E-11-F and allows the vector to be plotted. Clearing either the x or y position registers will also reset the blanking flip flop and allow points to be plotted after a vector has gone off screen and has set the blanking flip flop.

Other signals which inhibit the vector clock through OR gate $\overline{30}|$ D-16-R are: the PEN DOWN delay circuit, the circuit to limit the maximum pulse rate to the Cal-Comp plotter, and the CLOCK ENABLE flip flop, $\overline{30}|$ E-3. This CLOCK ENABLE flip flop is set by command bit 14 and a data strobe to begin a vector or curve, and is reset by an output from the main counter indicating the end of a vector, or by the all ones in a Δ register which indicates the completion of a $\frac{1}{4}$ circle arc.

Front panel controls permit the clock rate to be varied in the CRT mode and fix the rate at the maximum rate of the vector hardware in the plotter mode. The maximum rate of pulses to the plotter (300 pps) is limited by the plotter circuits.

Request-for-Data/Interrupts DS-1-33D

The inputs to the REQUEST-FOR-DATA circuit are shown on the left side of the drawing.

When loading the C. REG. the delayed command strobe is normally gated through |33 A-7-H, -J to generate the request after the command register has been loaded, unless inhibited by |33 A-8-L. When a command is loaded, specifying *x*, *y* and sign registers, event counters, S.P.E. or control switches as the data source, the request is inhibited and the delayed command strobe is gated to the data strobe input as described for the CLEAR-LOAD circuits DS-1-16D.

When a data strobe is issued and nothing is to be plotted (as indicated by an absence of command bits 14, 15, 16), the delayed data strobe is gated through |33 A-7-V, -U to produce a REQUEST-FOR-DATA after the registers have been loaded.

In displaying points or a single character, the display sends a RESUME pulse to the request circuits through |33 A-7-T, -S which generates a REQUEST-FOR-DATA. The display also issues a RESUME pulse for each point in a vector and each character in a 4-character group but these are inhibited by |33 A-8-H.

A REQUEST-FOR-DATA is generated after the fourth character by having the fourth character enable, from the vector-character control circuits, gate the RESUME pulse through |33 A-7-R, -P. When a vector is completed a REQUEST-FOR-DATA is generated by ANDing (|33 A-7-N, -M) command bit 14 with the change in level of the enable flip flop of the vector clock.

When points are plotted off screen or blanked by command bit 12, no point strobe is issued to the display and thus there will be no RESUME pulse from the display. The point strobe |29 E-22-U from a source not inhibited by blanking or an off-screen condition is used to generate the REQUEST-FOR-DATA in this case. This point strobe also occurs for each point of the vector and so must be inhibited by command bit 14 from raising a request when vectors are plotted. The request for blanked vectors is raised in the normal manner by the vector clock enable flip flop when the vector is completed.

The REQUEST-FOR-DATA from the ALL 0 DATA = CEU circuits was previously described under the description of the CLEAR-LOAD circuits.

The foregoing inputs are used to initiate a pulse from |33 A-7-D which sets flip flop |33 A-5 to produce a UNIT READY/BUFFER READY signal to the 840A. The flip flop is set to the not-ready state when it receives a data or command strobe from the 840A or, if it is in the external memory mode (command bit 8), after a delay of approximately

1.2 μsec as provided by |33 A-6-M. The flip flop may also be set to the ready state by a manual clear switch, an initial condition generator (ICG) or the initial condition bus (ICB) from the 840A. The ICG provides a level to clear the flip flop for several seconds after power is initially switched on.

When the display processor is operating in the memory mode with command bit 8 set, the UNIT READY/BUFFER READY signal is given to the 840A for only 1.2 μsec and a delay (|33 A-6-V) of 5 μsec is triggered. If the computer is waiting to use the display processor it will 'see' the 1.2-μsec ready signal and be able to issue a new command word which removes bit 8 before 5 μsec. This will restore control to the 840A. If the 840A does not respond to the 1.2-μsec ready signal the memory will receive a REQUEST-FOR-DATA pulse after 5 μsec and will issue the next word.

The REQUEST-FOR-DATA will raise an interrupt to the 840A if |33 A-3-R has been enabled by '1 group B of the command register. An interrupt will also be raised when the event counter reaches zero if |33 A-3-T has been enabled by flip flop |33 A-4-E. This flip flop is enabled by '3 group B and disabled by '2 group B of the command register.

The output of level changer 33| B-1-R indicates to the external memory that the display processor is not operating in the memory mode.

Connectors DS-1-40D

This drawing shows connections between the display processor and the external devices. For those connectors associated with one drawing the drawing number is indicated in brackets below the connector name. For connectors which connect to circuits on more than one drawing, the drawing numbers are shown in the angle symbol.

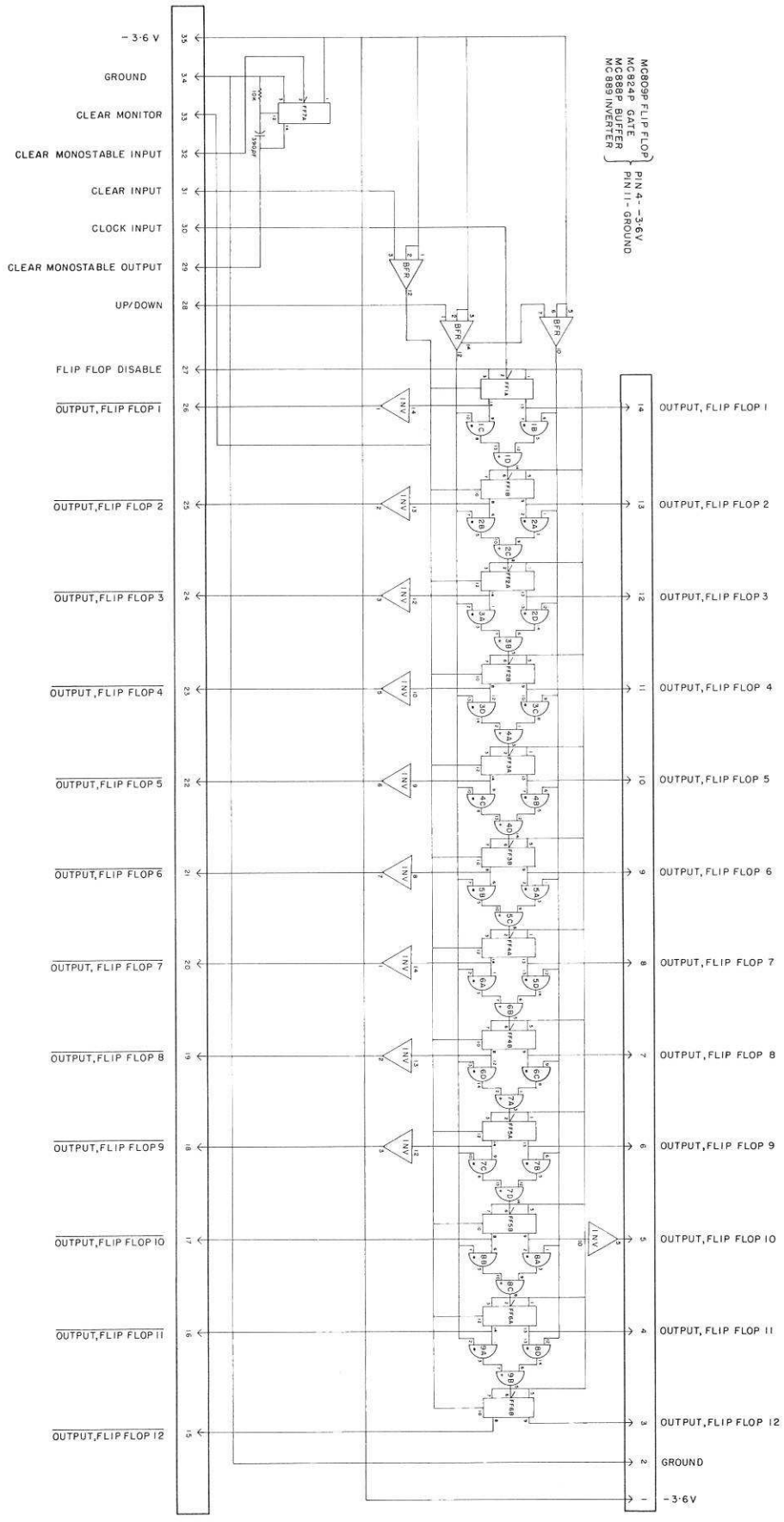
References

1. Pulfer, J.K. Digital display hardware for man–machine communication studies. Bulletin of Canadian Information Processing Society, 8 (6): 18–23; 1968.

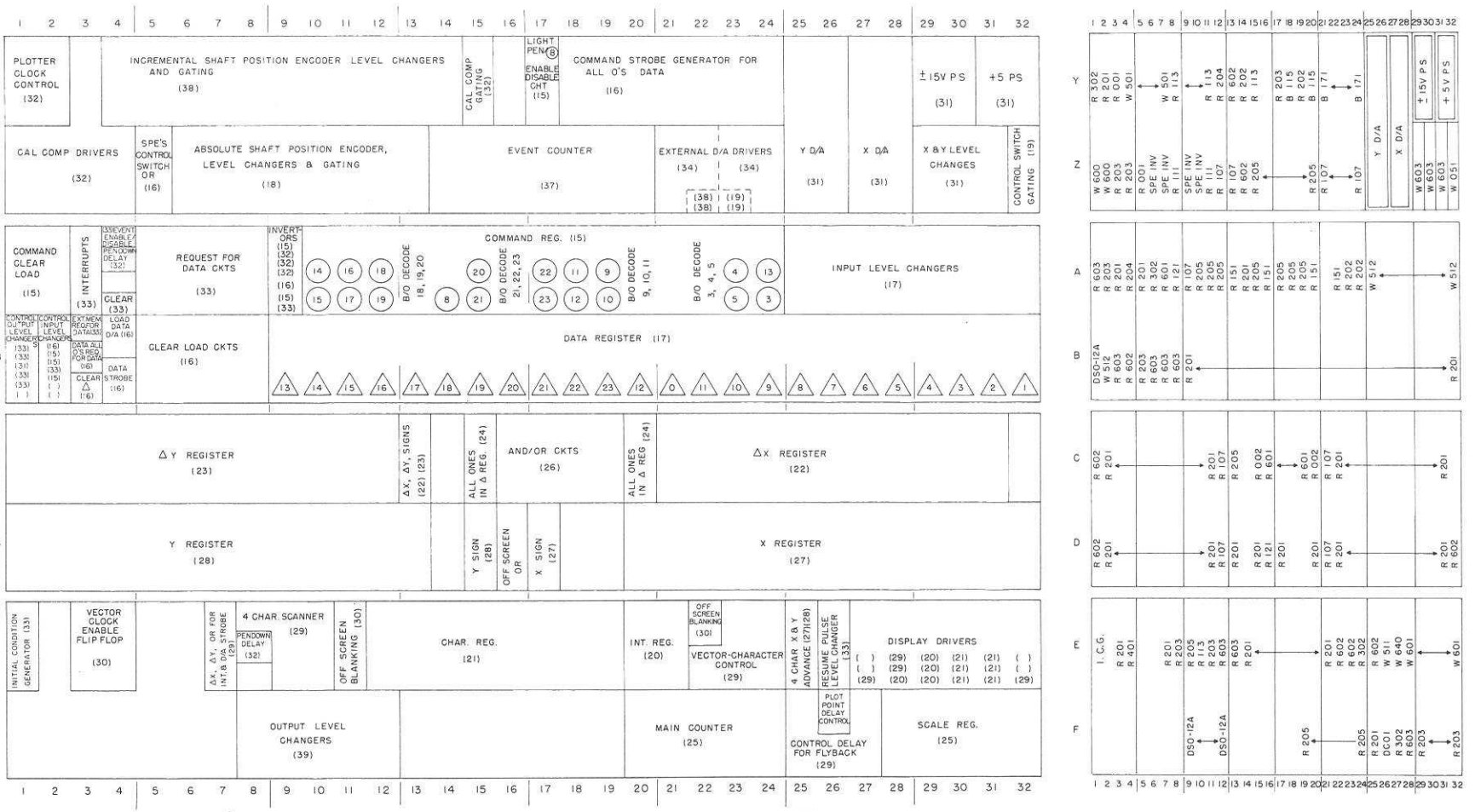
2. Pulfer, J.K. Programmers Reference Manual for Digital CRT Display. NRC Rept. Radio and Electrical Engineering Division ERB-788, 1968.

3. Digital Equipment Corporation. Digital Logic Handbook, Flip Chip Modules, 1967.

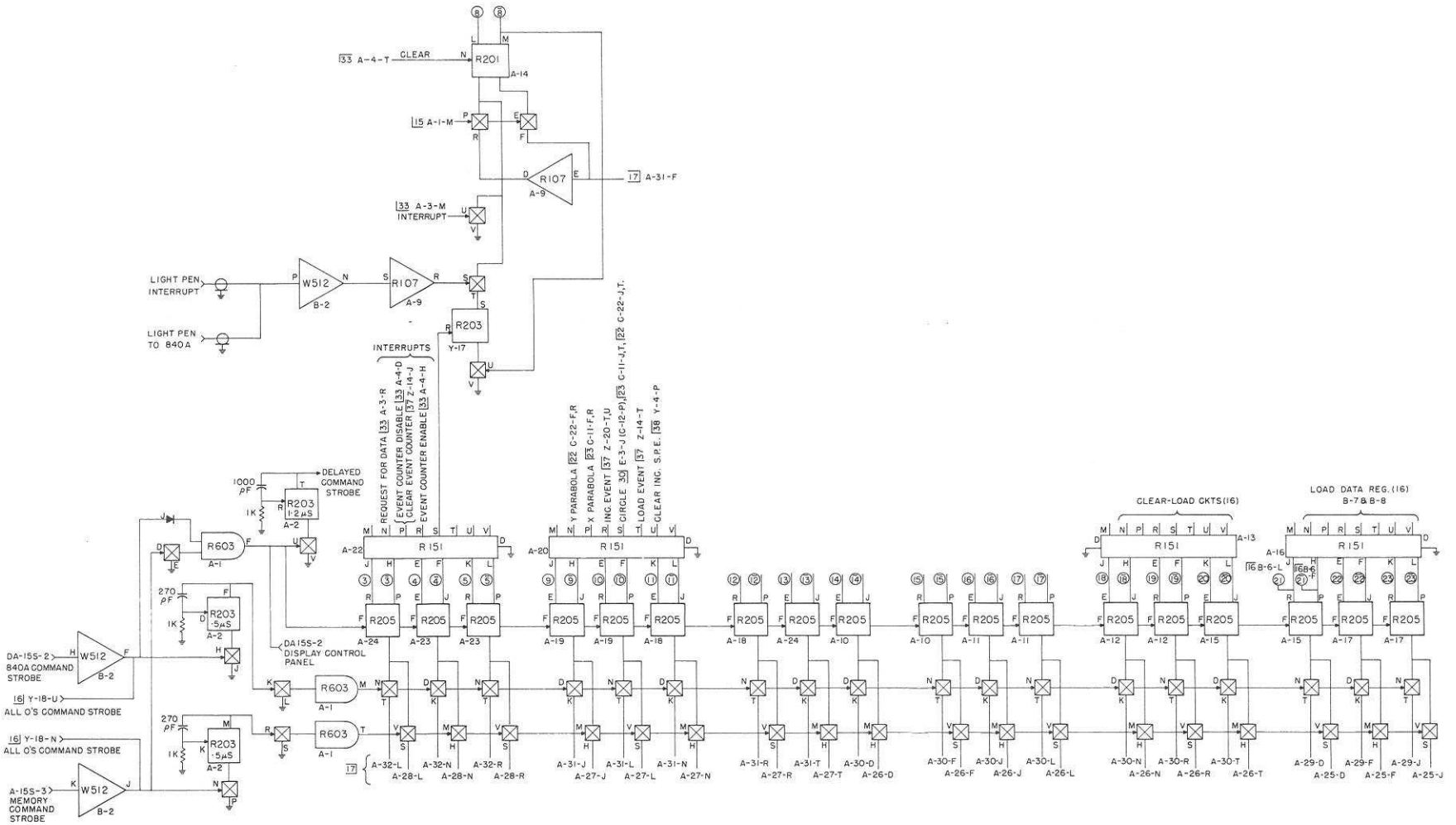
4. Polzen, K.P. Line generator using binary rate multiplier techniques. NRC Rept. Radio and Electrical Engineering Division ERB-747, 1966.



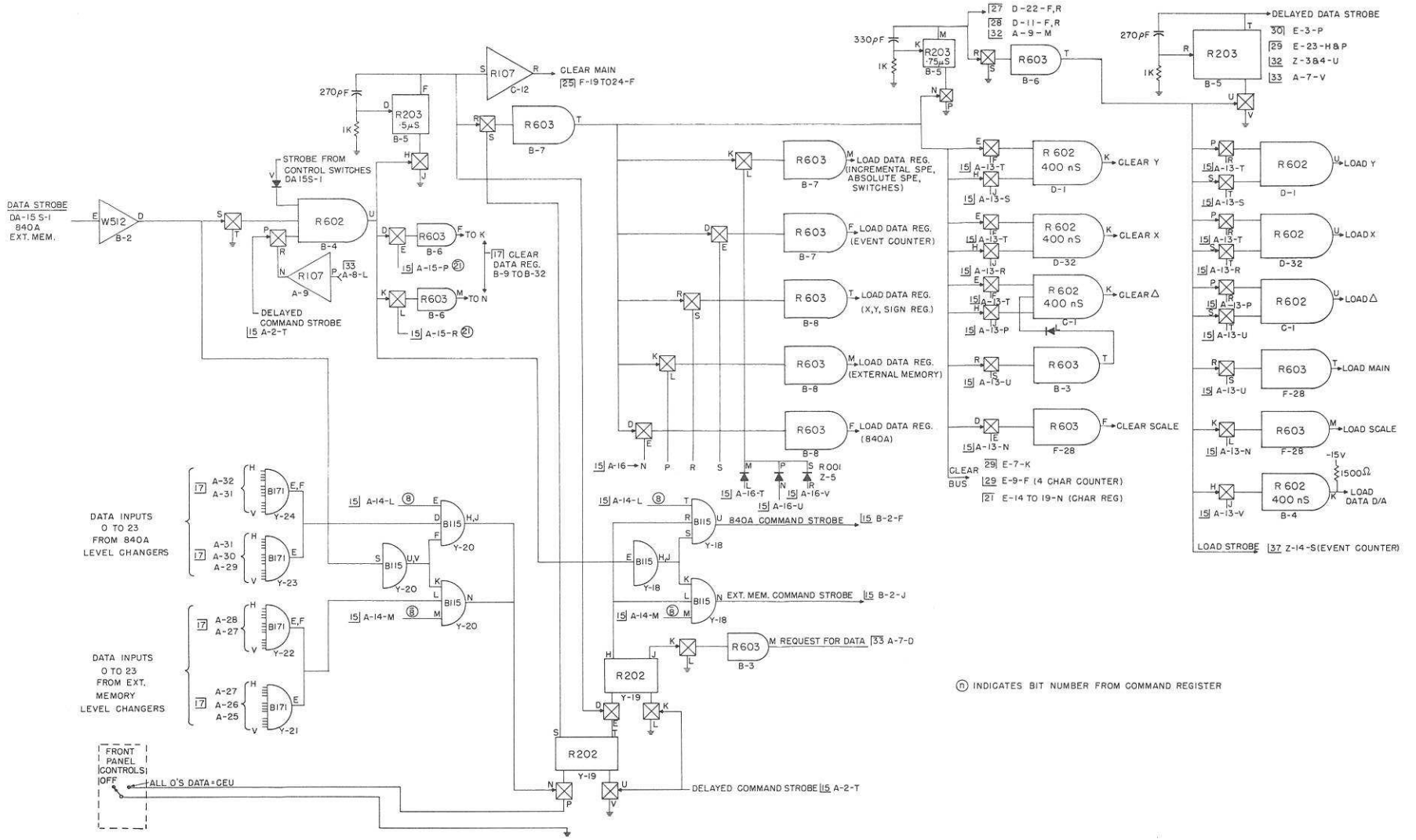
Drawing No. DS-0-9D. Up/down counter (12 bit)



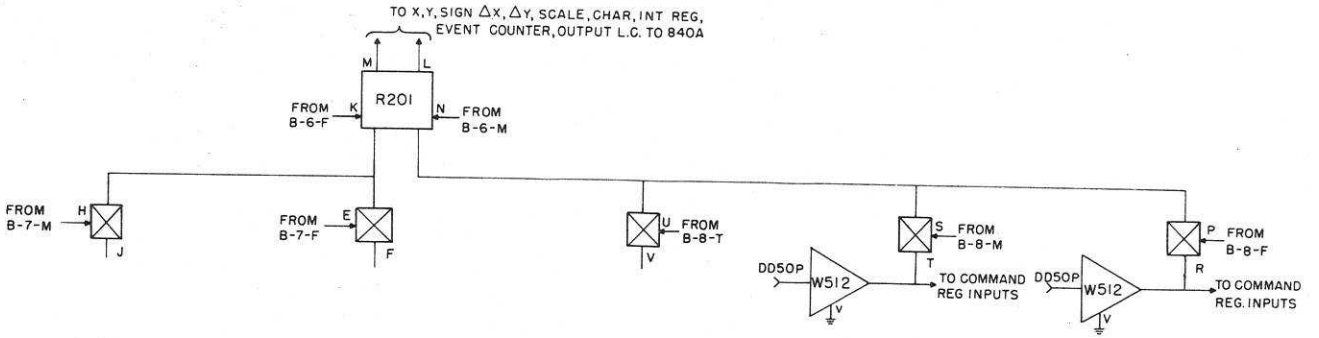
Drawing No. DS-1-14D. Circuit board functions and locations



Drawing No. DS-1-15D. Command register



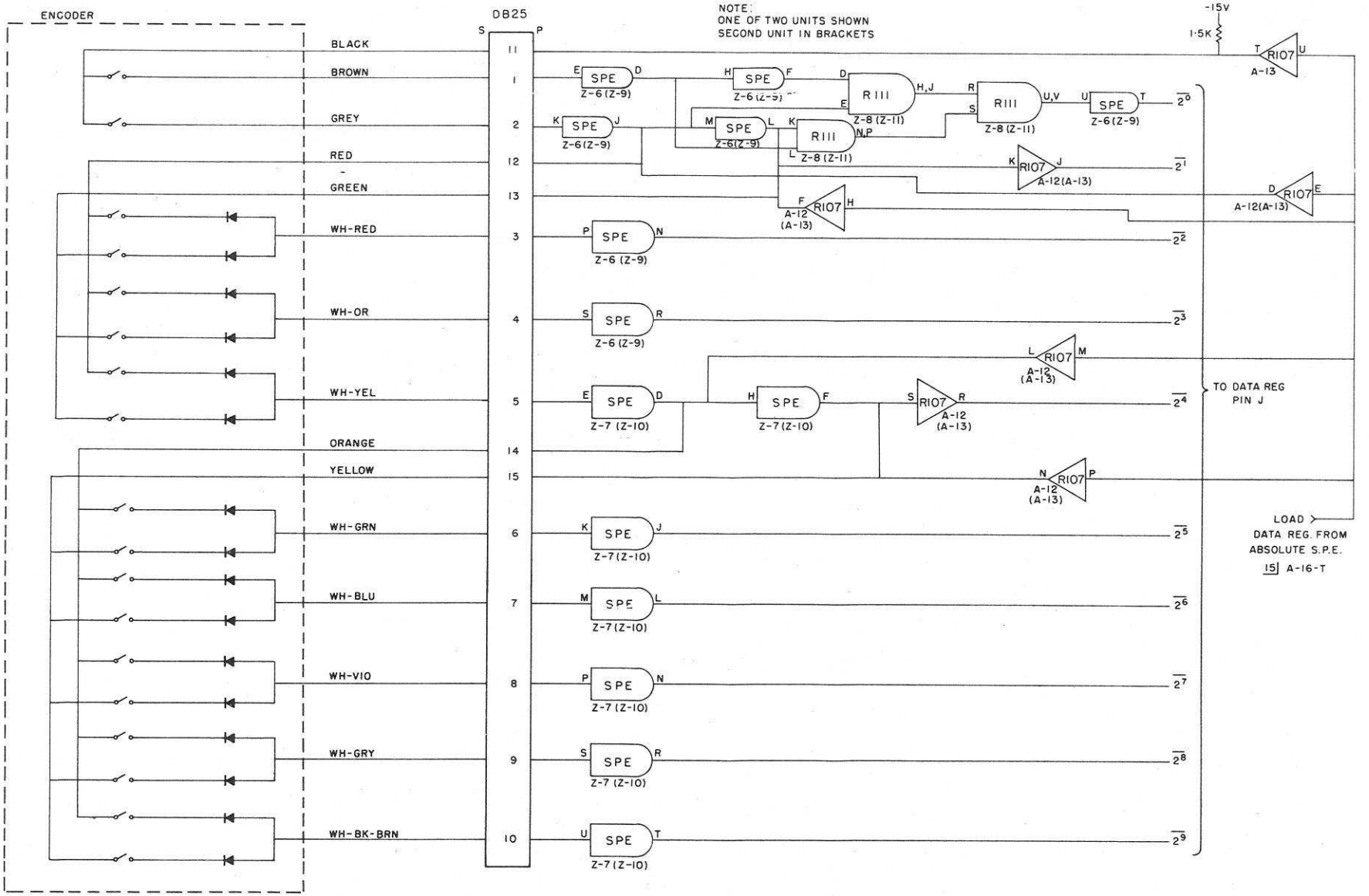
Drawing No. DS-1-16D. Clear-load circuits



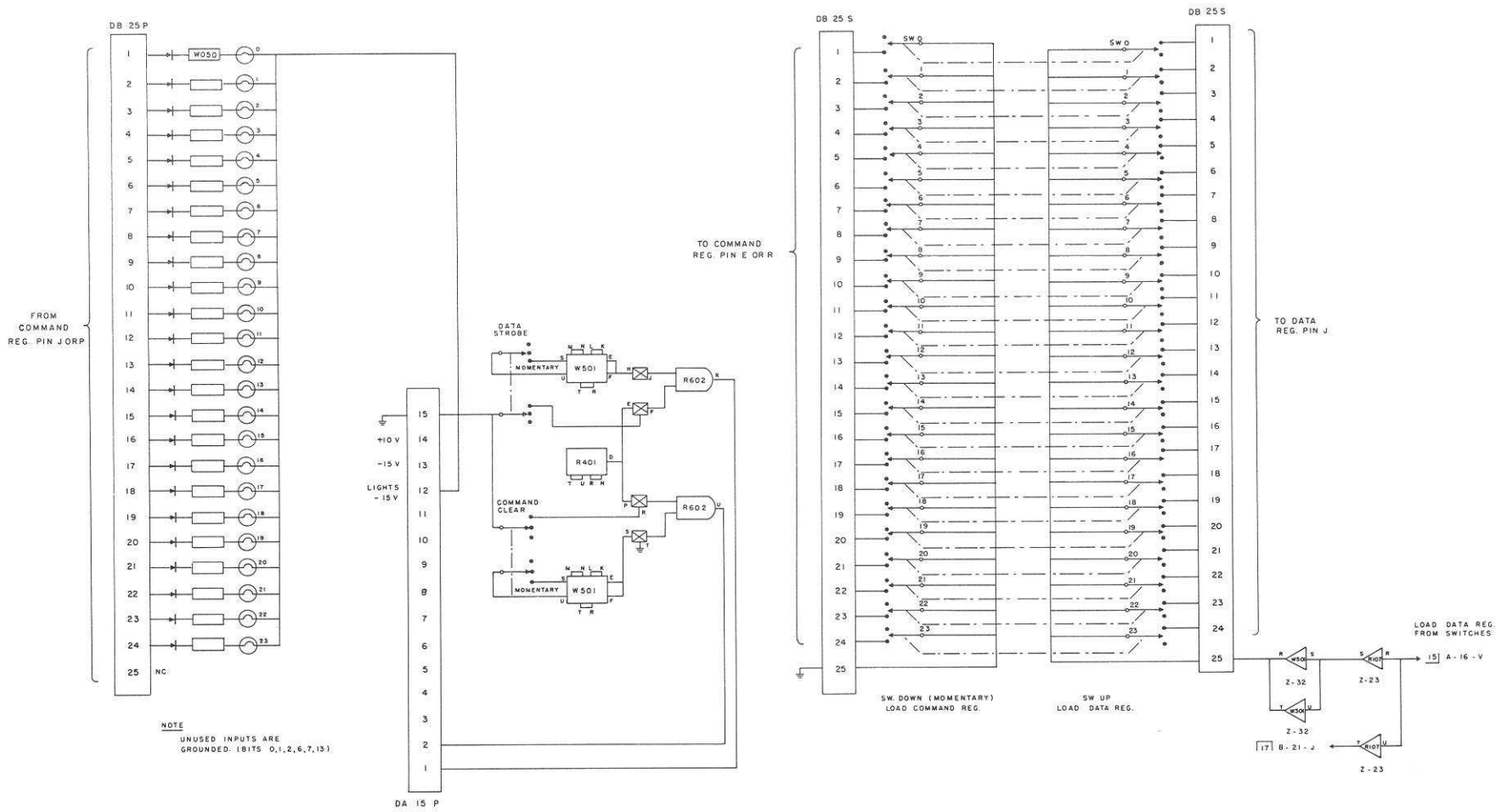
BIT	DATA REG LOCATION	INC S.P.E.(38)	ABSOLUTE S.P.E. (18)	SW'S (19) DA25P	EVENT COUNTER (37)	FROM X,Y, SIGN REG(27,28,22,23)
0	B-21	19 Z-14-T	19 Z-14-T	1	GND	D-17-M
1	B-32	Y-15-F	A-10-T	2	GND	D-31-M
2	B-31	Y-15-K	A-10-R	3	GND	D-30-M
3	B-30	Y-15-N	A-10-N	4	GND	D-29-M
4	B-29	Y-15-S	A-10-L	5	GND	D-28-M
5	B-28	Y-15-V	A-10-J	6	GND	D-27-M
6	B-27	Y-16-F	Z-13-R	7	GND	D-26-M
7	B-26	Y-16-K	A-9-R	8	GND	D-25-M
8	B-25	Y-16-N	A-9-N	9	GND	D-24-M
9	B-24	Y-16-S	Z-13-J	10	GND	D-23-M
10	B-23	Y-16-V	A-9-T	11	GND	D-22-M
11	B-22	——	——	12	GND	C-13-R
12	B-20	——	——	13	Z-15-J	D-15-M
13	B-9	Y-13-F	A-7-T	14	Z-15-P	D-2-M
14	B-10	Y-13-K	A-7-R	15	Z-16-J	D-3-M
15	B-11	Y-13-N	A-7-N	16	Z-16-P	D-4-M
16	B-12	Y-13-S	A-7-L	17	Z-17-J	D-5-M
17	B-13	Y-13-V	A-7-J	18	Z-17-P	D-6-M
18	B-14	Y-14-F	Z-12-R	19	Z-18-J	D-7-M
19	B-15	Y-14-K	A-6-R	20	Z-18-P	D-8-M
20	B-16	Y-14-N	A-6-N	21	Z-19-J	D-9-M
21	B-17	Y-14-S	Z-12-J	22	Z-19-P	D-10-M
22	B-18	Y-14-V	A-6-T	23	Z-20-J	D-11-M
23	B-19	——	——	24	Z-20-P	C-13-E

EXT MEM CONNECTOR LEVEL CHANGER				840 A CONNECTOR LEVEL CHANGER		
	INPUT		OUTPUT		INPUT	OUTPUT
1	A-28-E	D	1	A-32-E		D
2	A-28-H	F	2	A-32-H		F
3	A-28-K	J	3	A-32-K		J
4	A-28-M	L	4	A-32-M		L
5	A-28-P	N	5	A-32-P		N
6	A-28-S	R	6	A-32-S		R
7	A-28-U	T	7	A-32-U		T
8	A-27-E	D	8	A-31-E		D
9	A-27-H	F	9	A-31-H		F
10	A-27-K	J	10	A-31-K		J
11	A-27-M	L	11	A-31-M		L
12	A-27-P	N	12	A-31-P		N
13	A-27-S	R	13	A-31-S		R
14	A-27-U	T	14	A-31-U		T
15	A-26-E	D	15	A-30-E		D
16	A-26-H	F	16	A-30-H		F
17	A-26-K	J	17	A-30-K		J
18	A-26-M	L	18	A-30-M		L
19	A-26-P	N	19	A-30-P		N
20	A-26-S	R	20	A-30-S		R
21	A-26-U	T	21	A-30-U		T
22	A-25-E	D	22	A-29-E		D
23	A-25-H	F	23	A-29-H		F
24	A-25-K	J	24	A-29-K		J

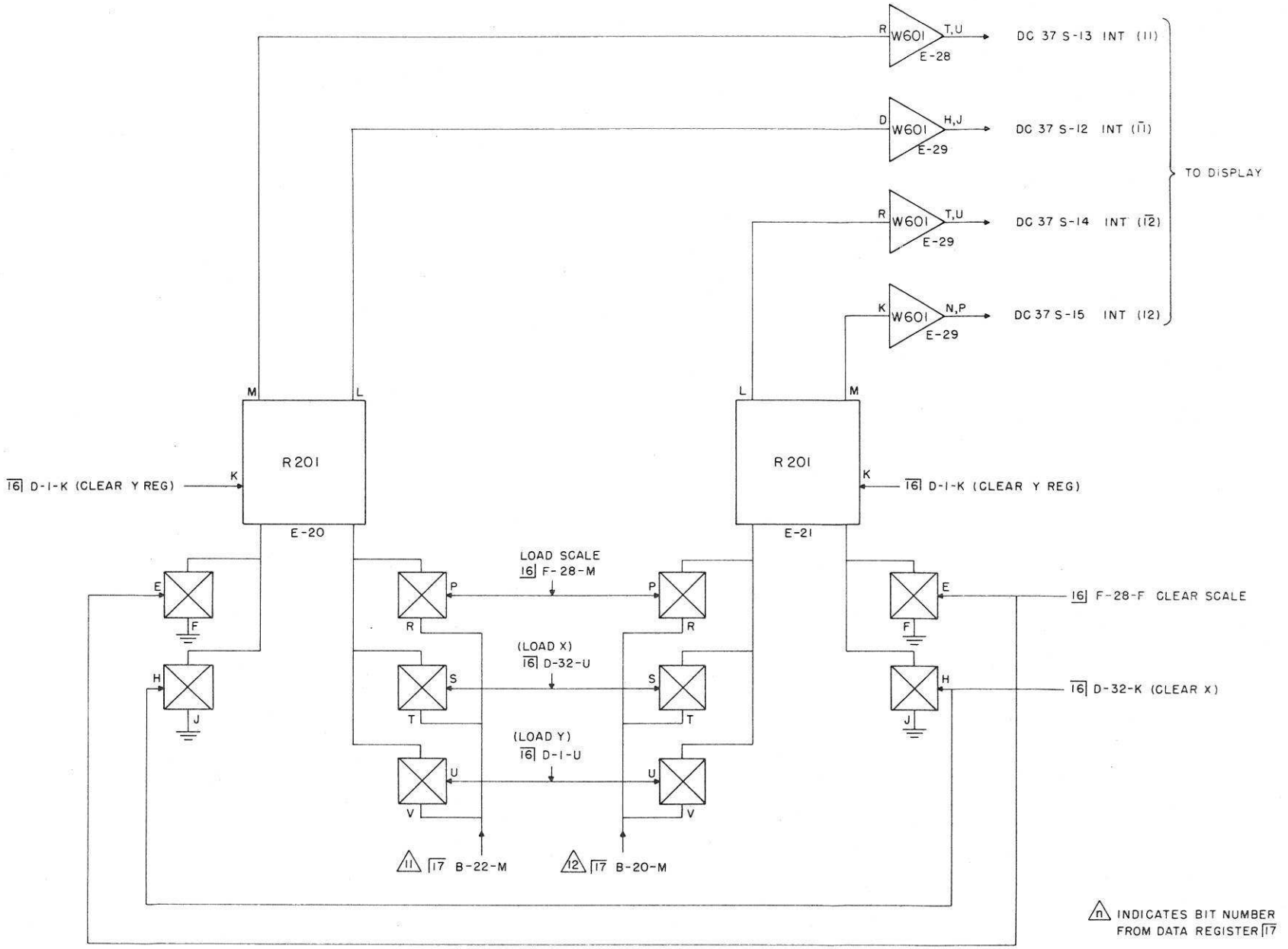
Drawing No. DS-1-17D. Data register



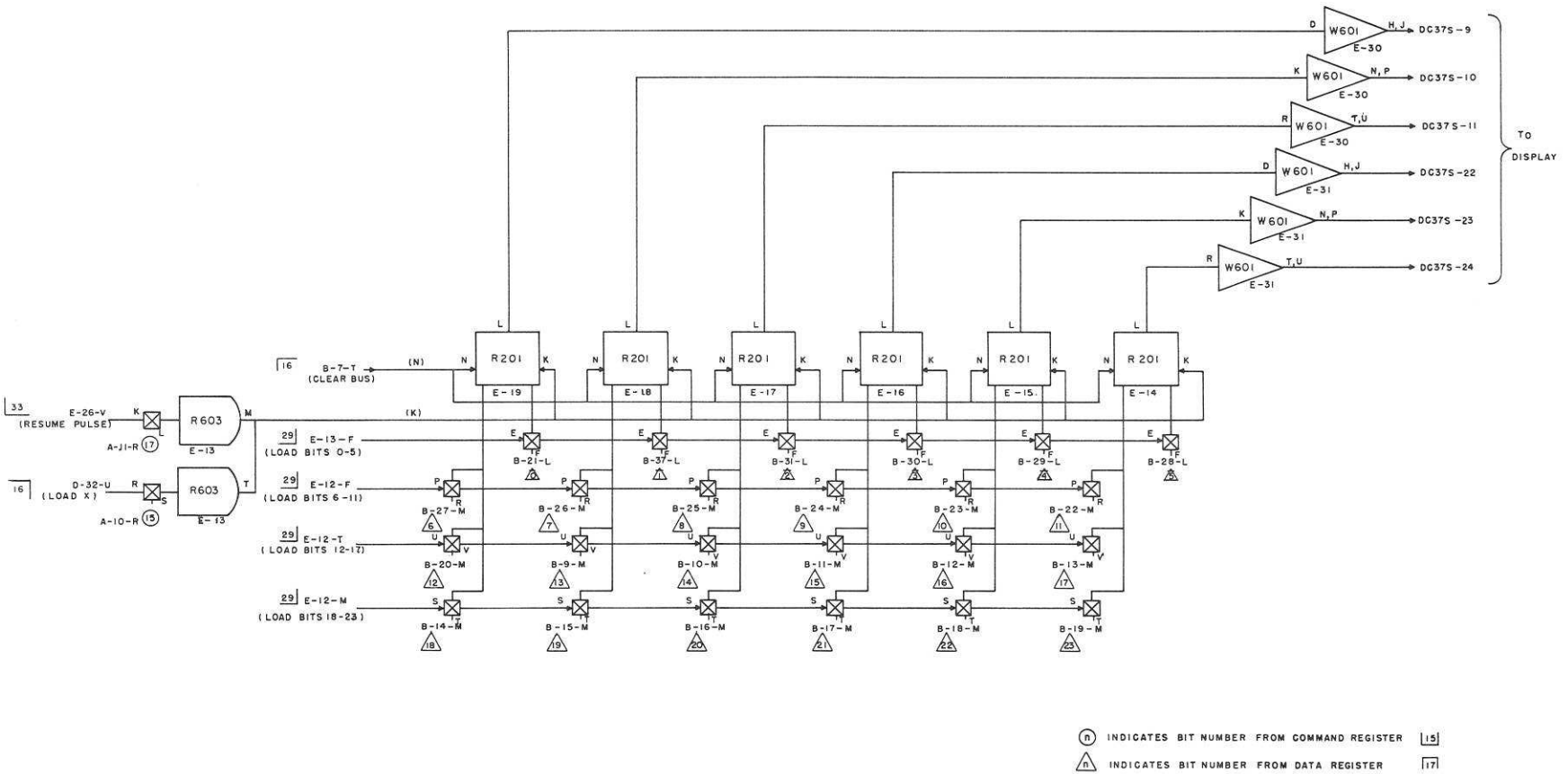
Drawing No. DS-1-18D. Absolute shaft position encoders



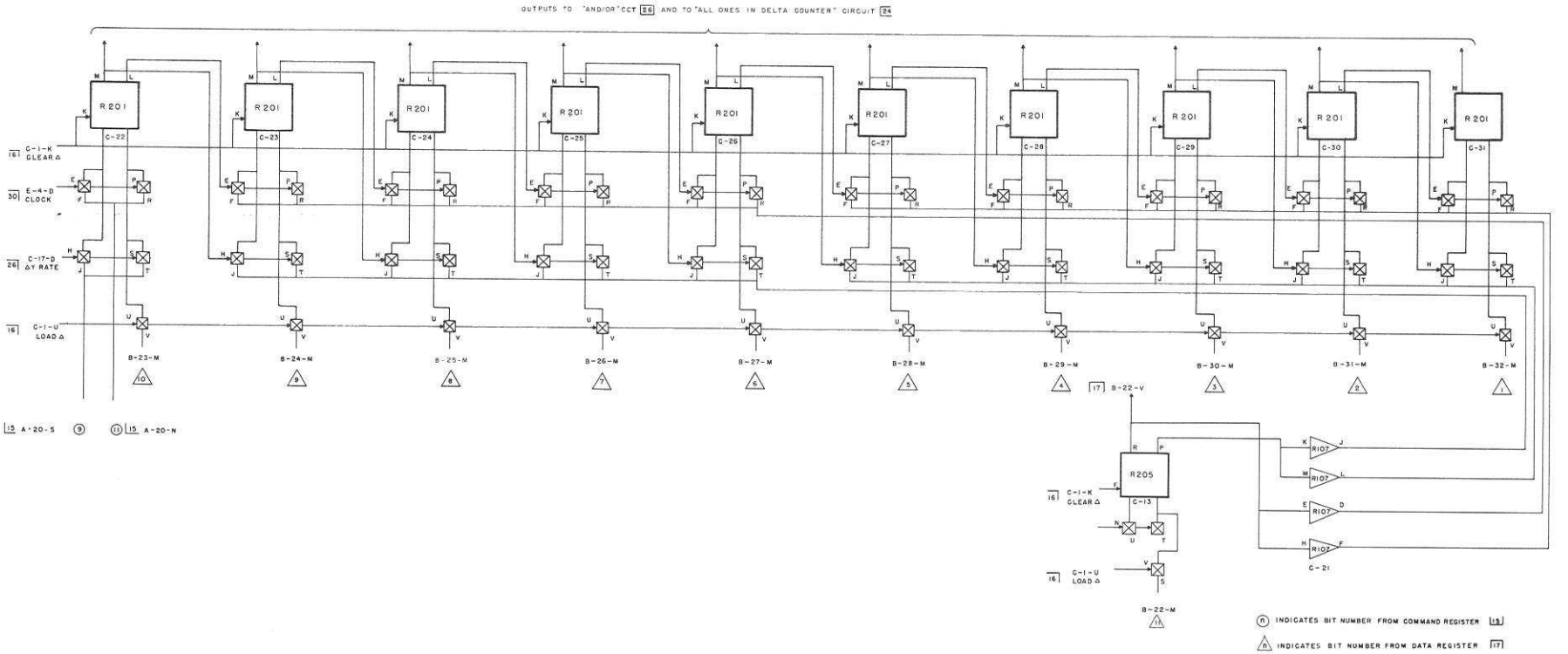
Drawing No. DS-1-19D. Control switch panel



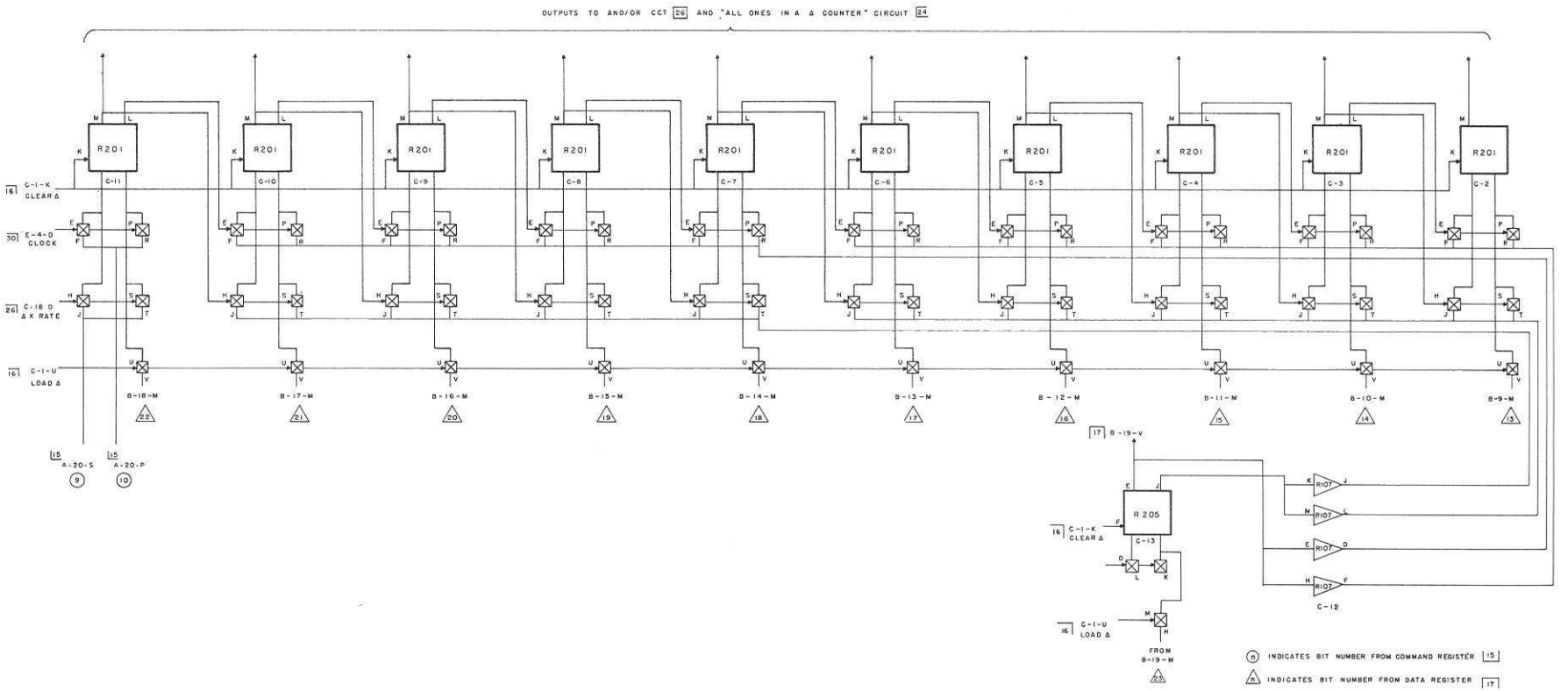
Drawing No. DS-1-20D. Intensity register



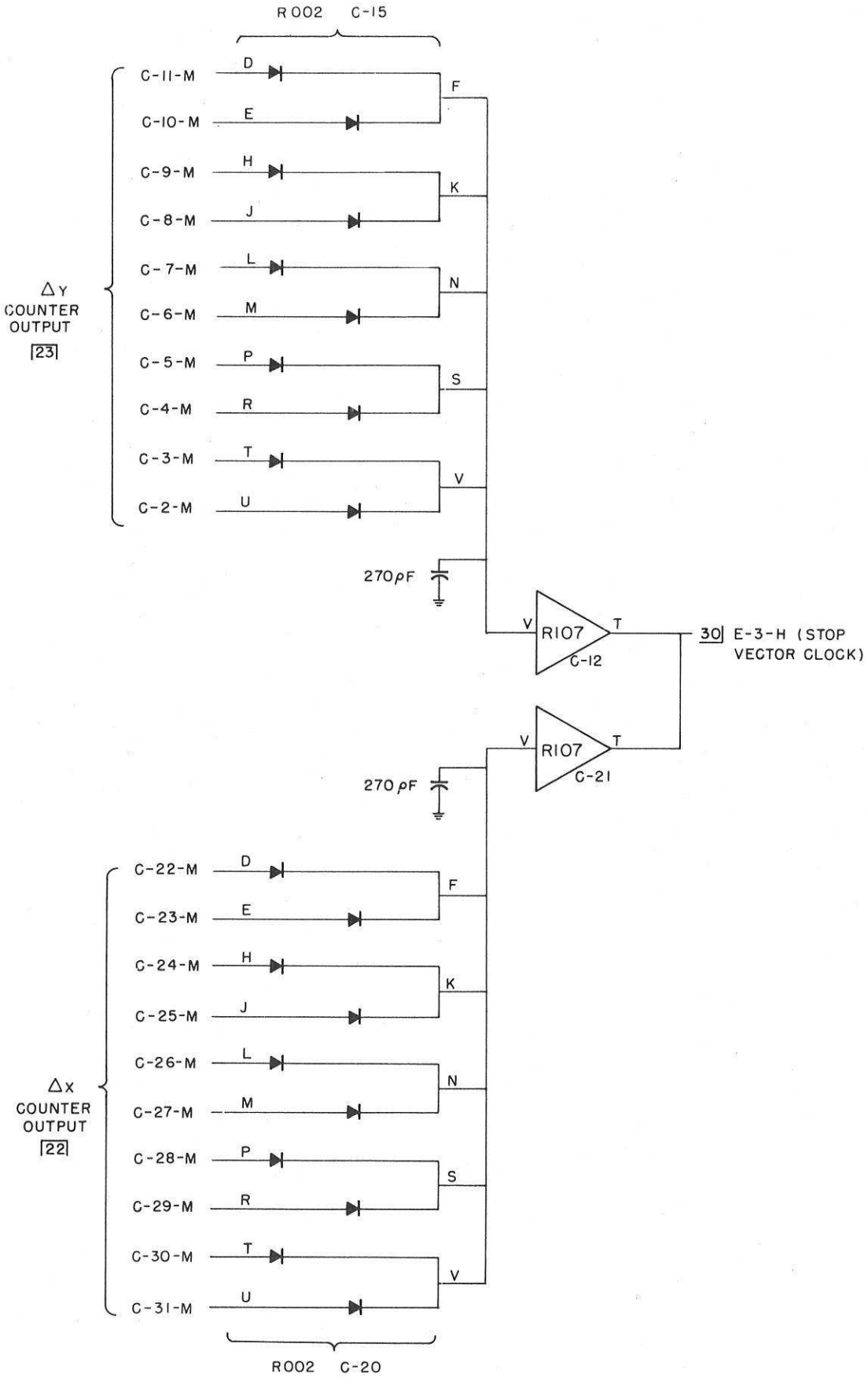
Drawing No. DS-1-21D. Character register



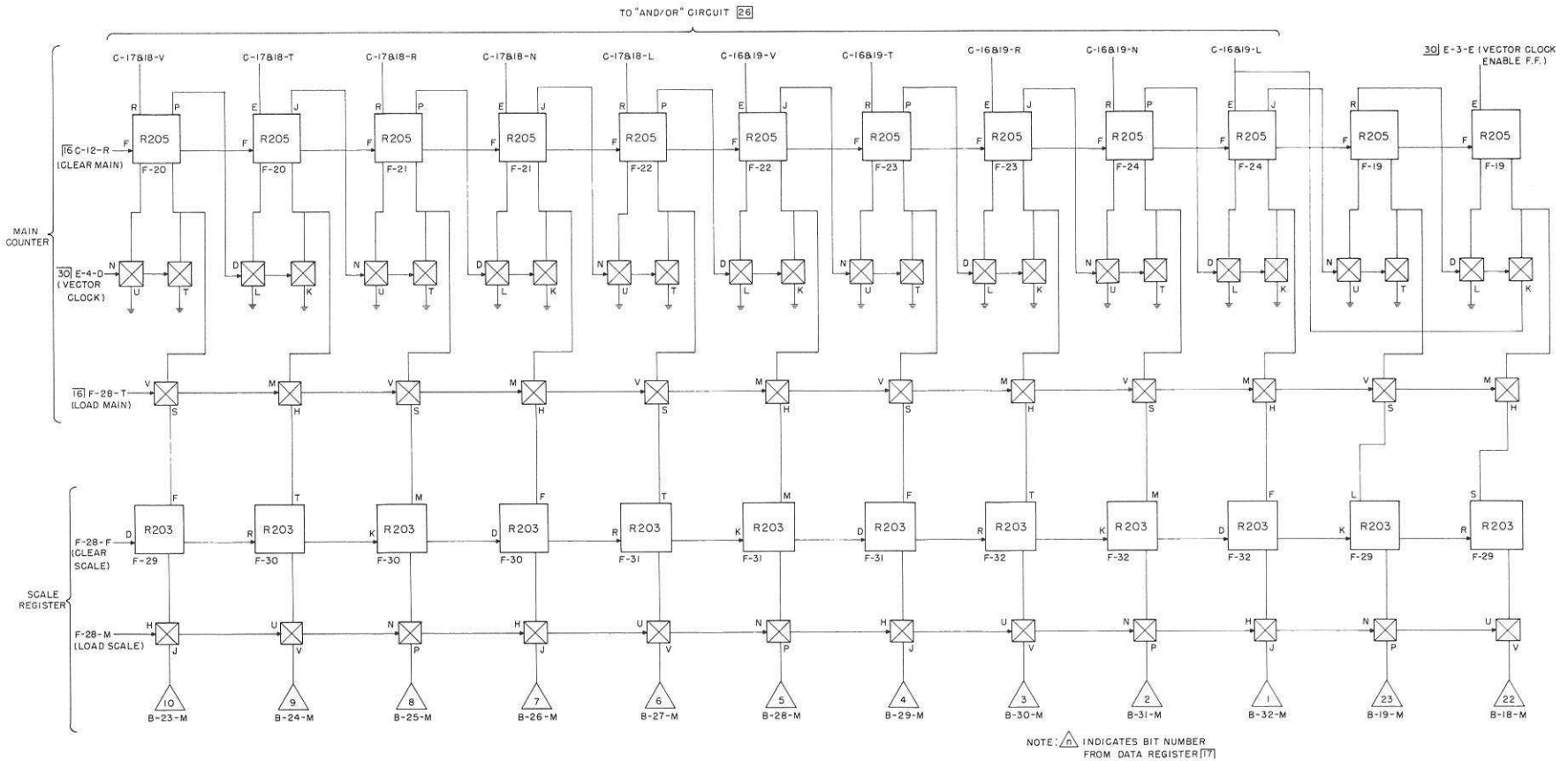
Drawing No. DS-1-22D. Δx counter



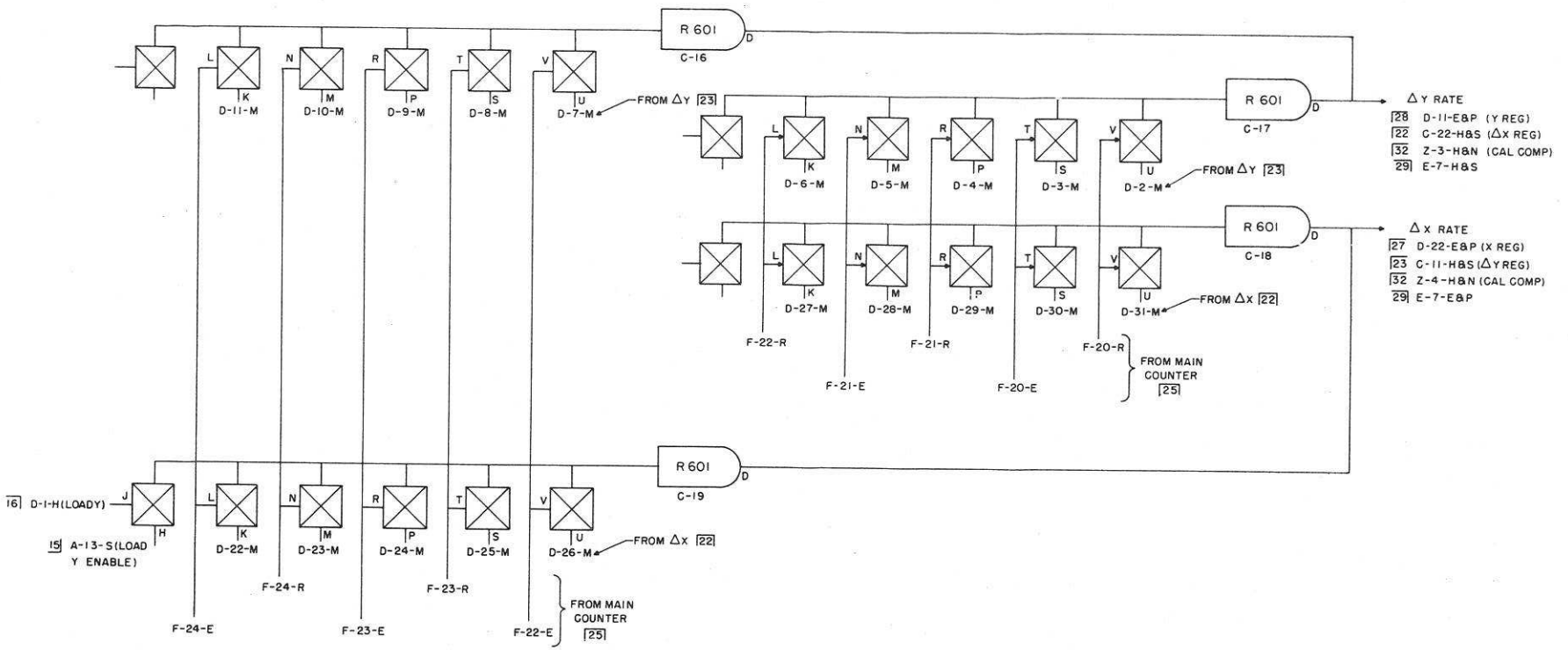
Drawing No. DS-1-23D. Δy counter



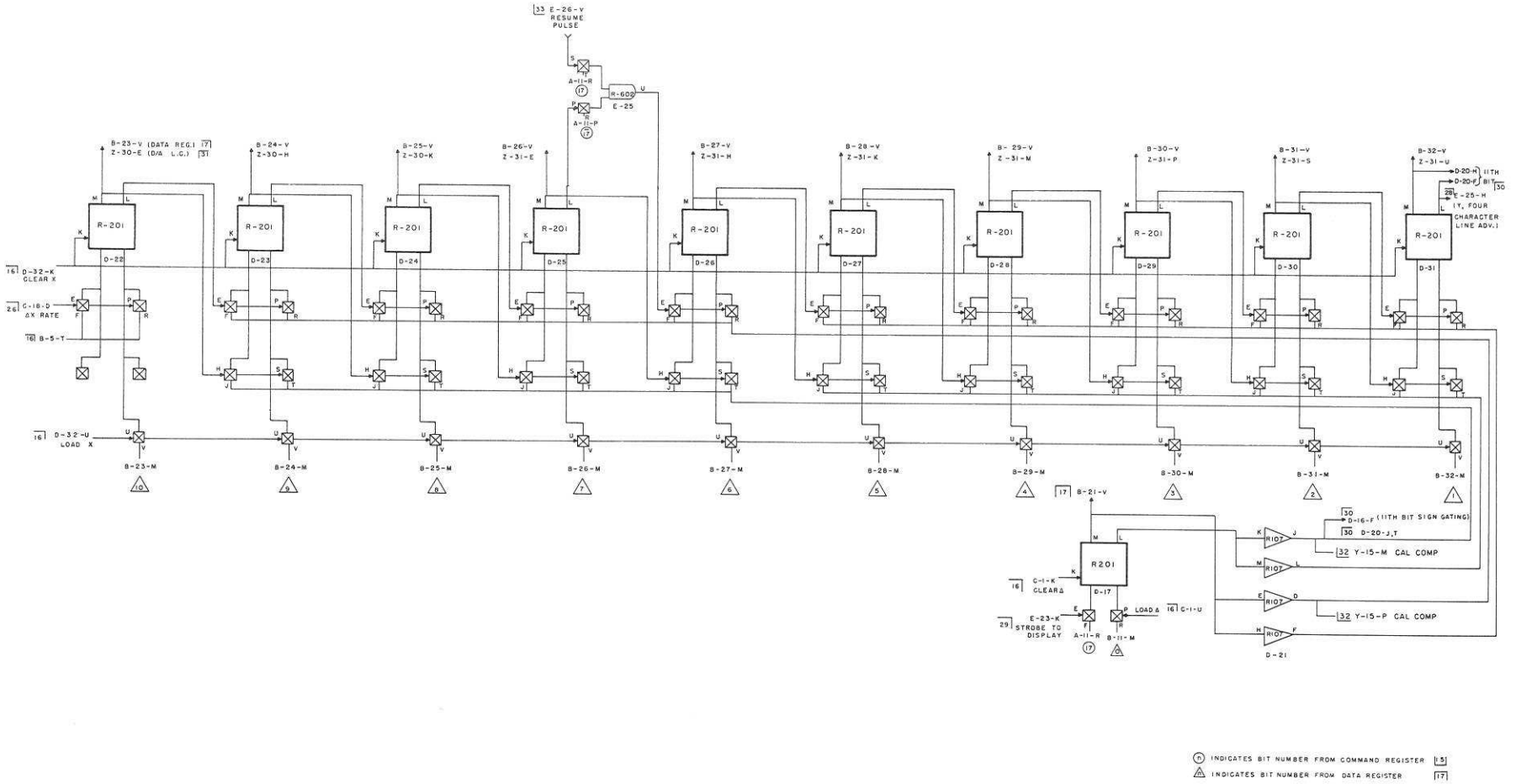
Drawing No. DS-1-24D. All ones in a Δ register



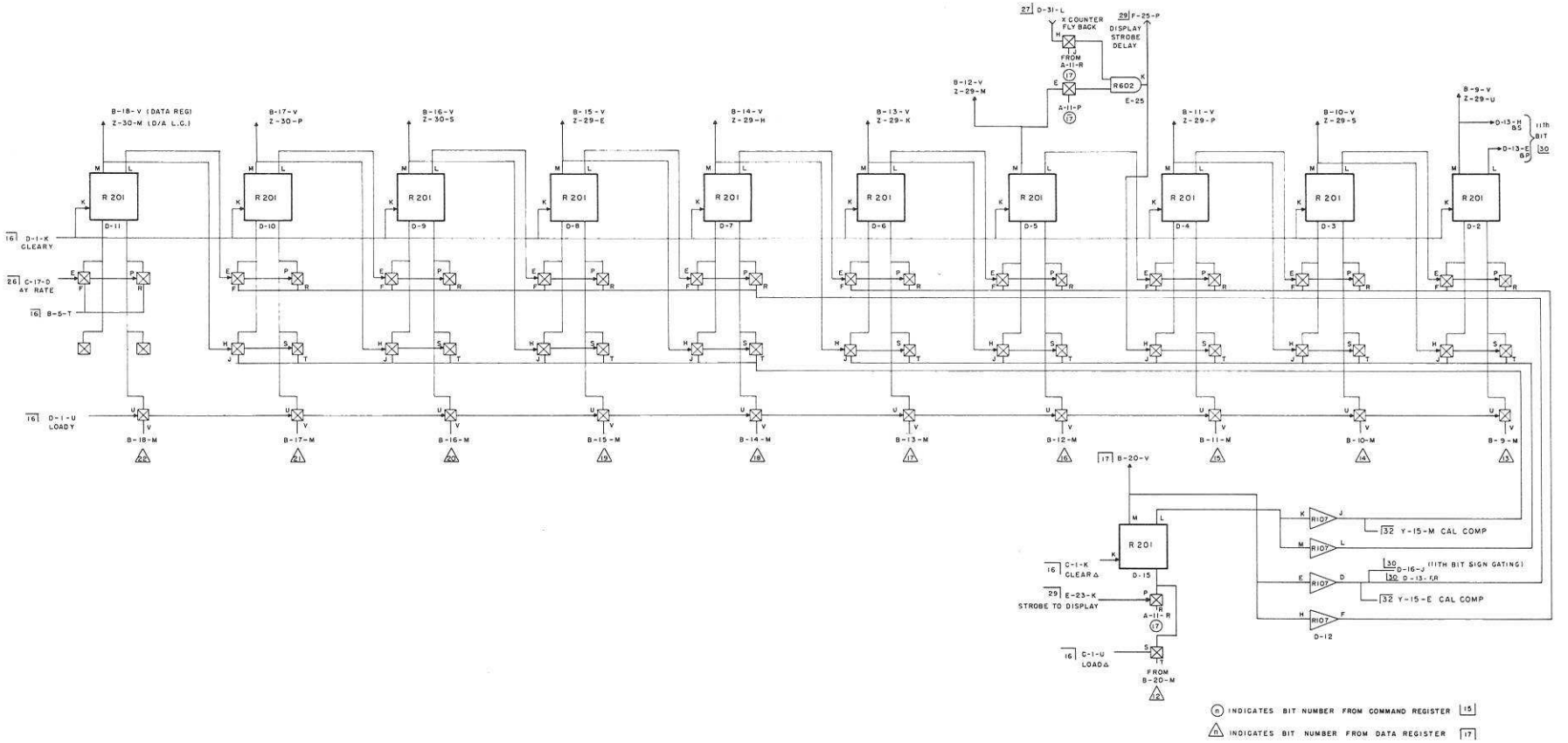
Drawing No. DS-1-25D. Main counter scale register



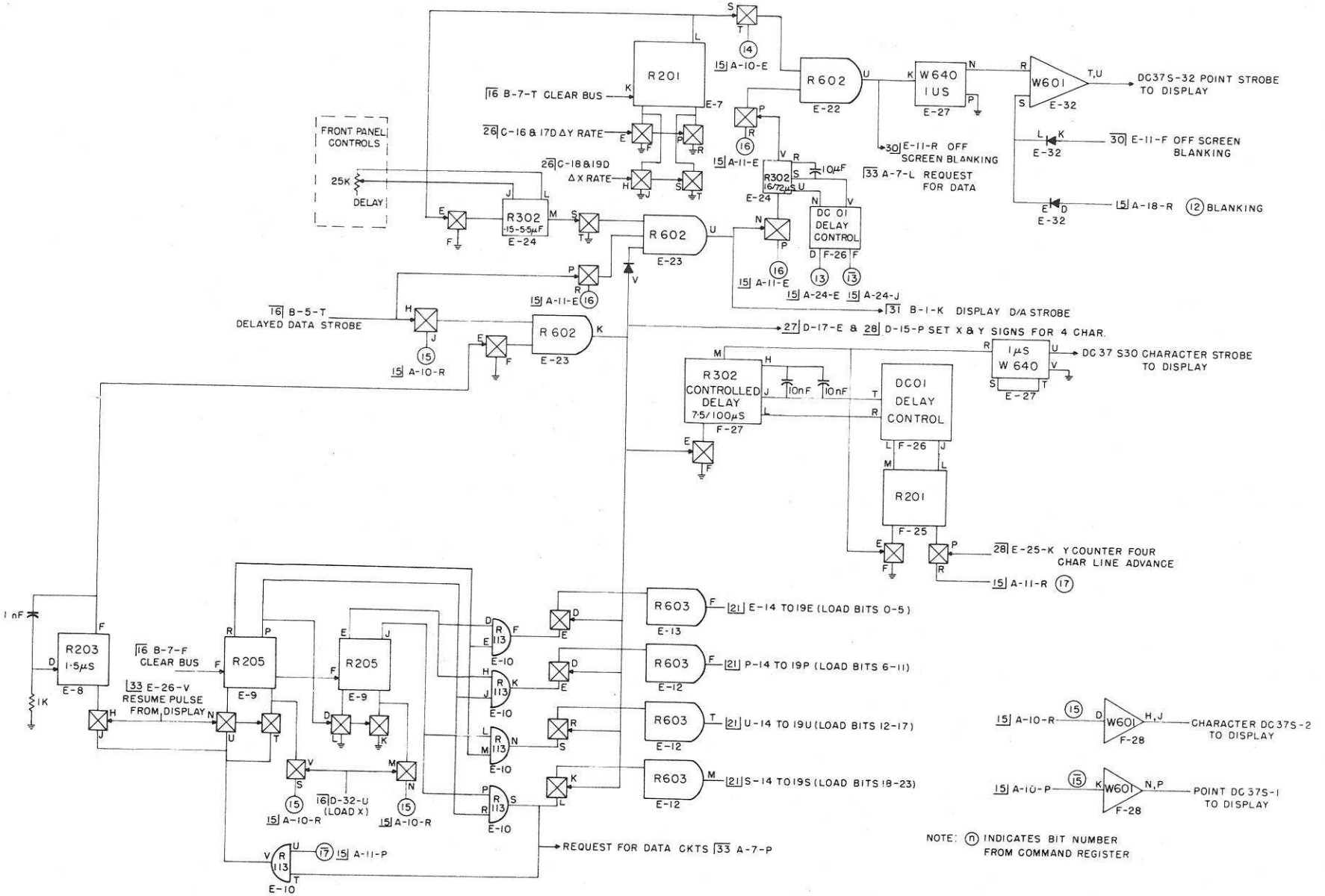
Drawing No. DS-1-26D. 'And/or' circuit



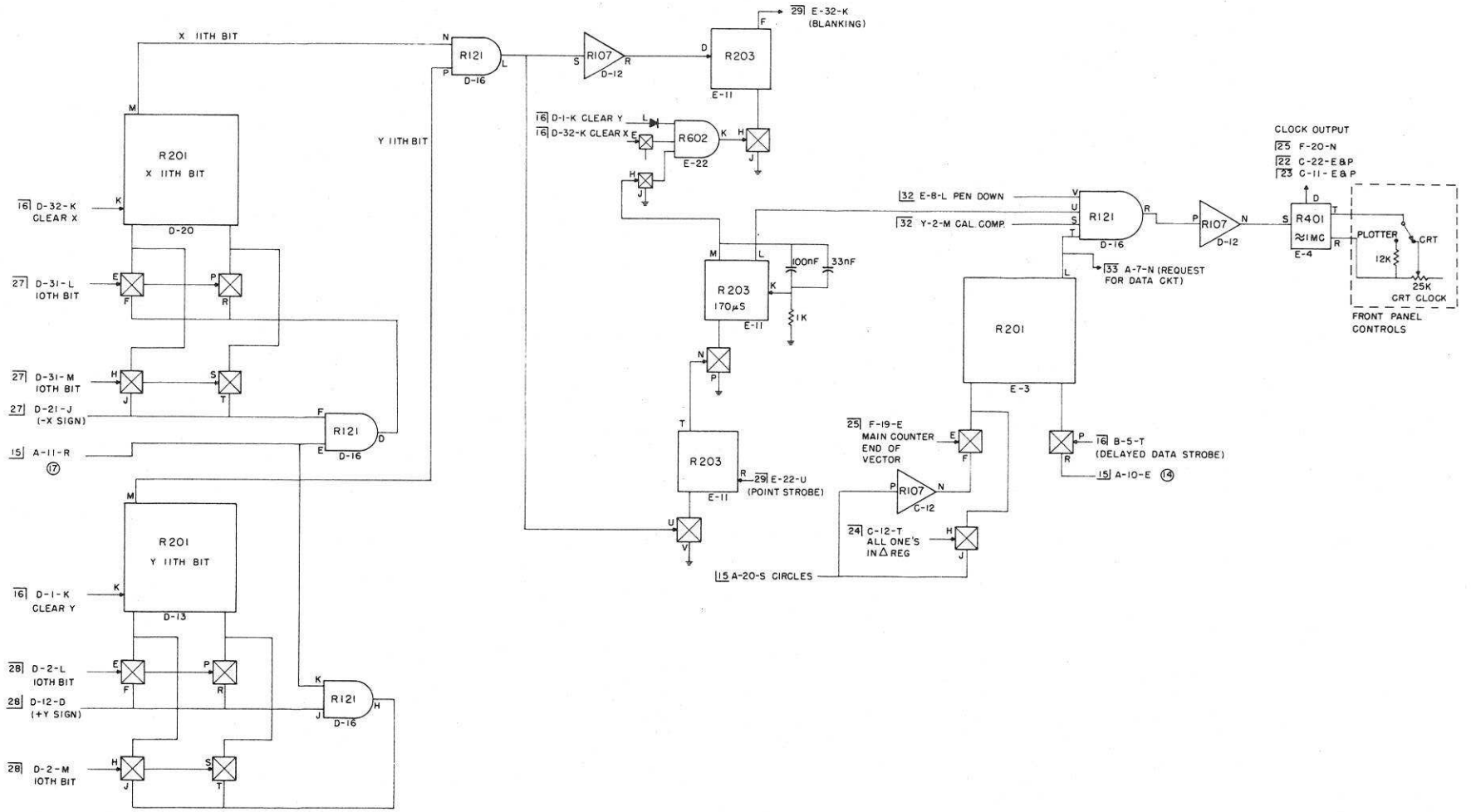
Drawing No. DS-1-27D. x counter/register



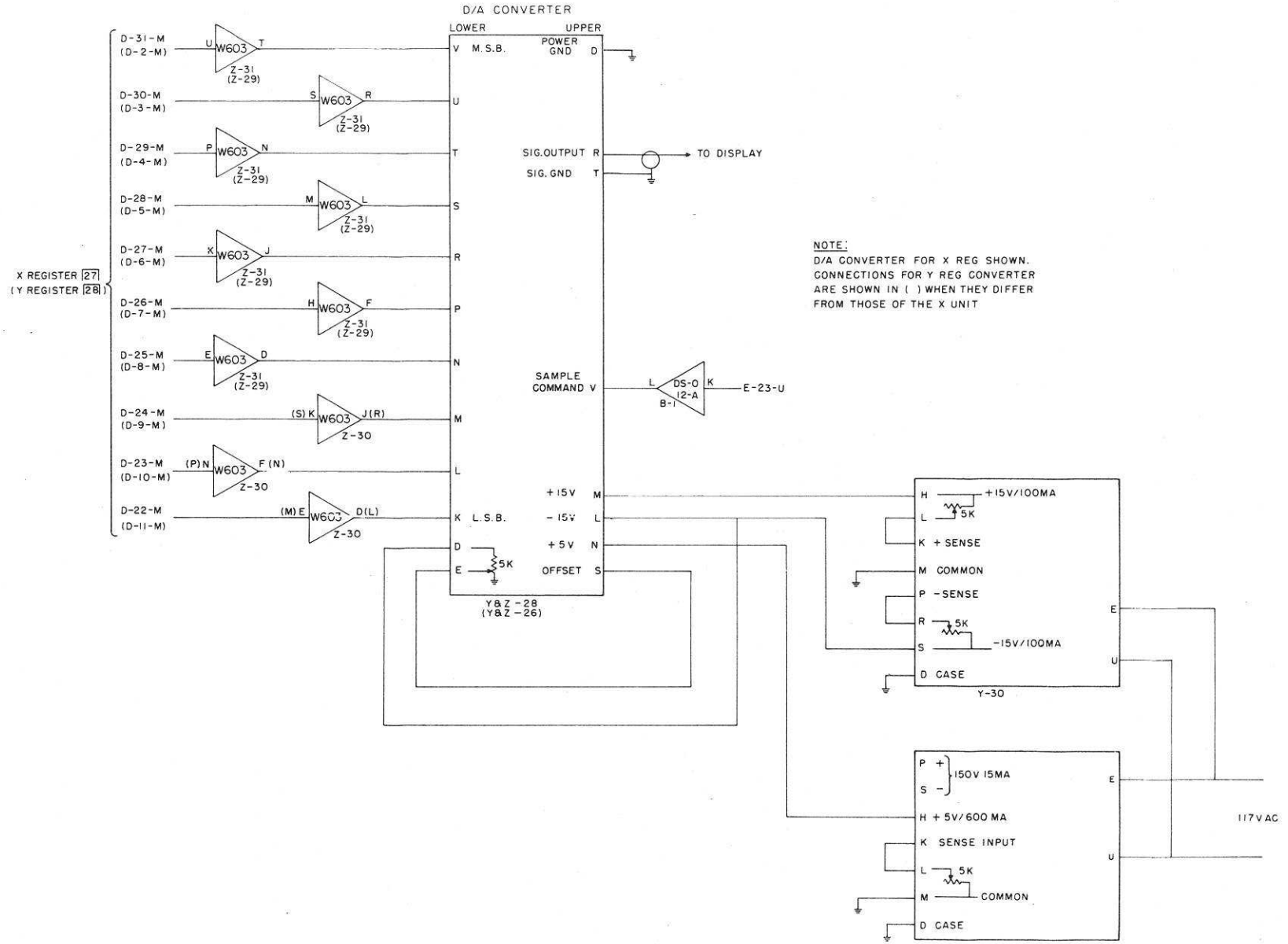
Drawing No. DS-1-28D. y counter/register



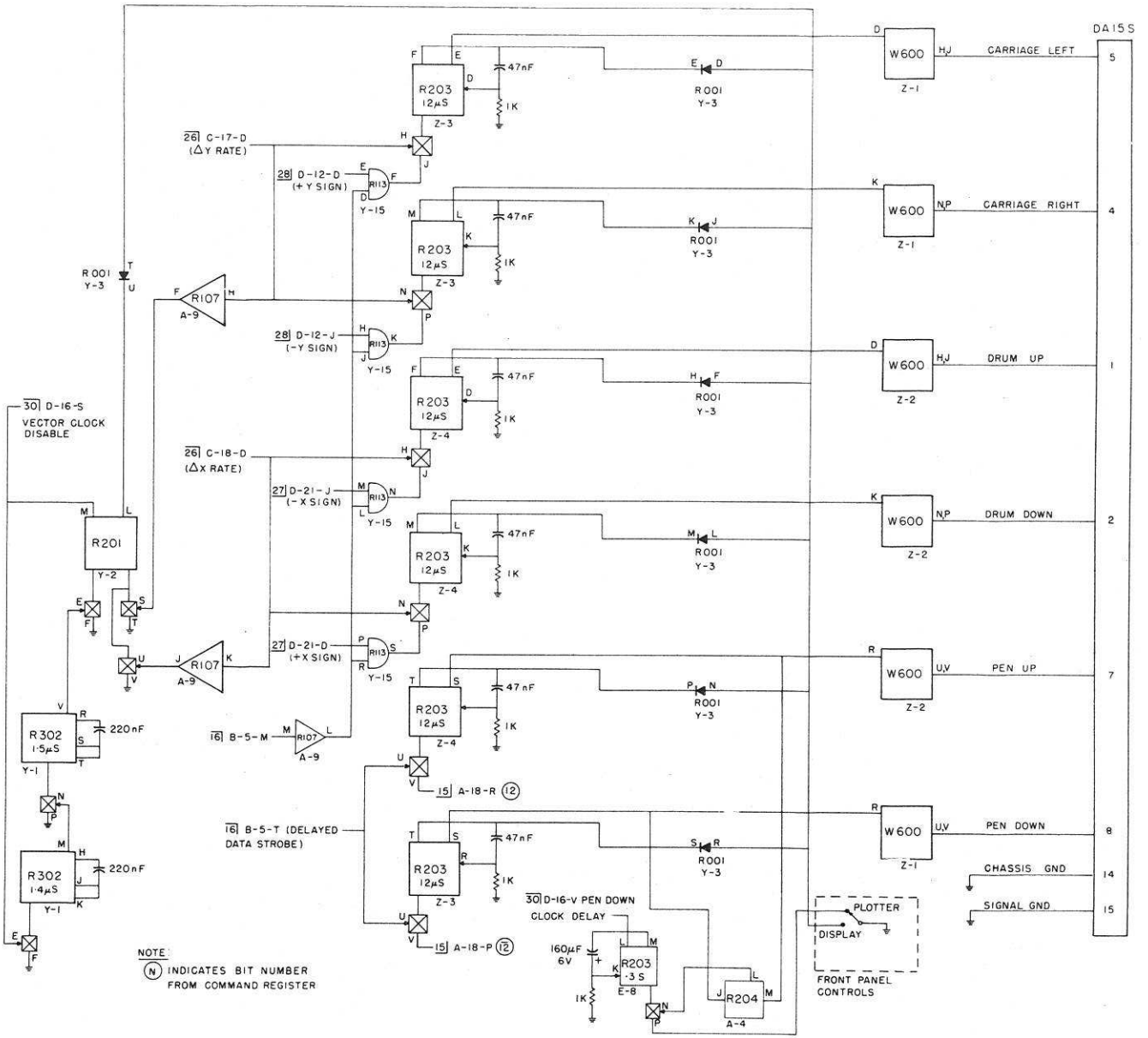
Drawing No. DS-1-29D. Vector-character control



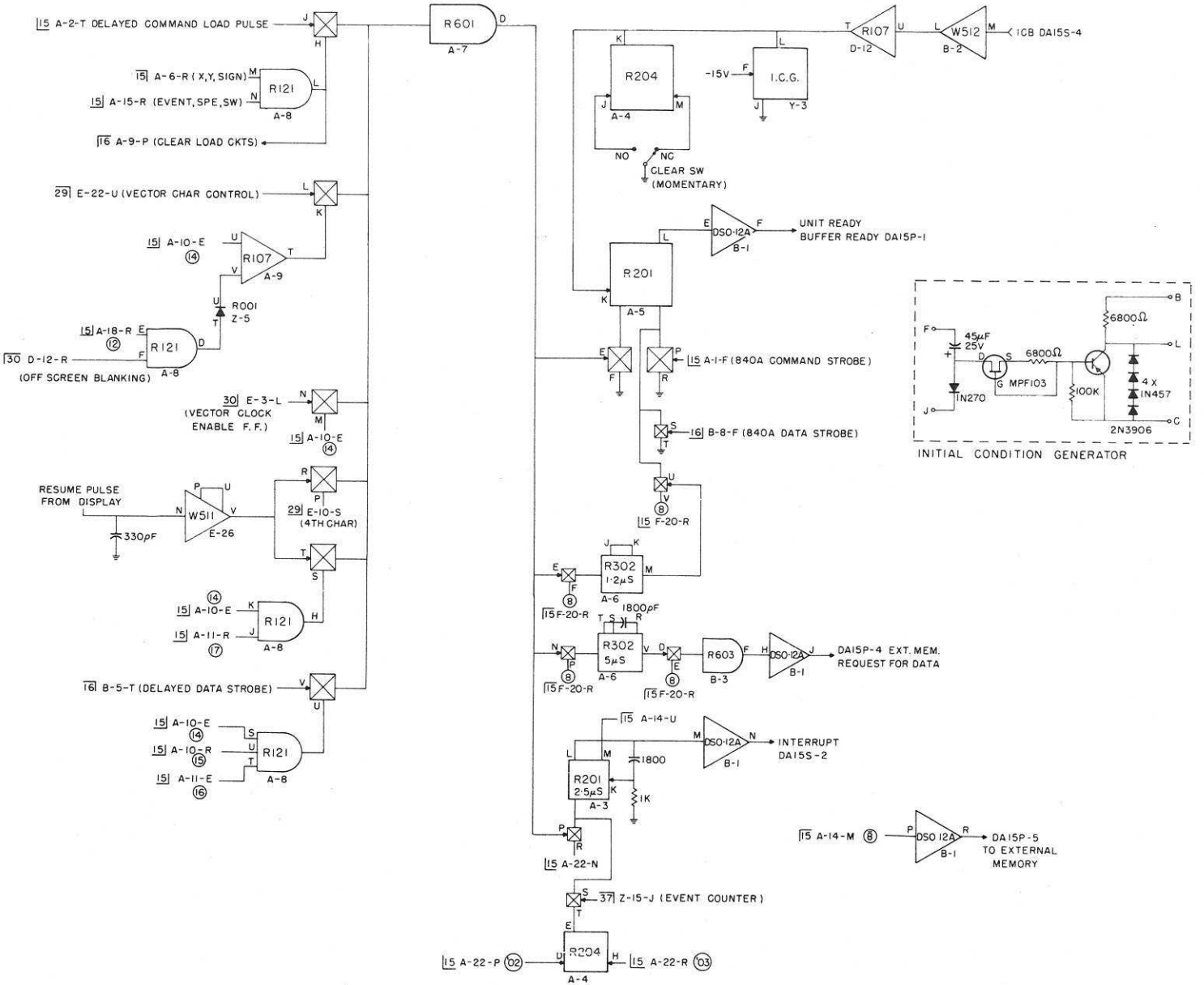
Drawing No. DS-1-30D. Off screen blanking



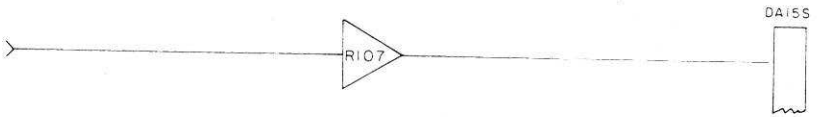
Drawing No. DS-1-31D. Display D/A converters



Drawing No. DS-1-32D. Cal-comp drivers

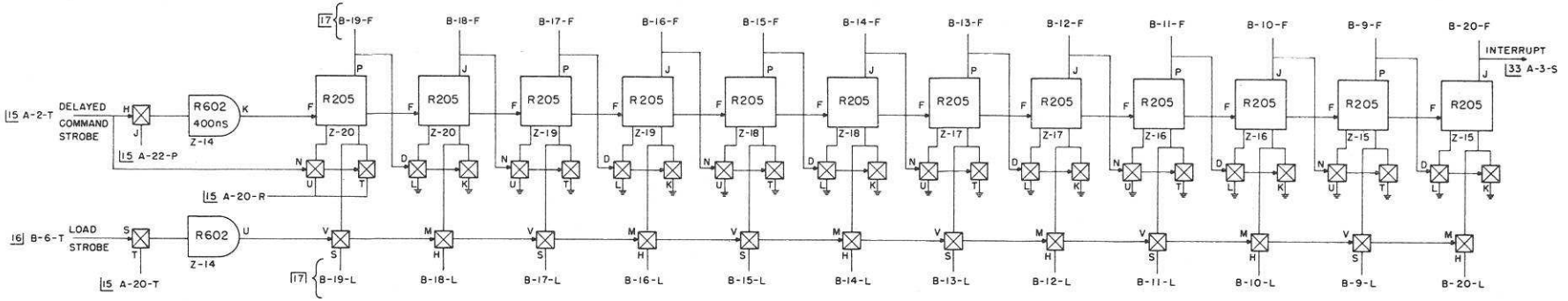


Drawing No. DS-1-33D. Request for data/interrupts

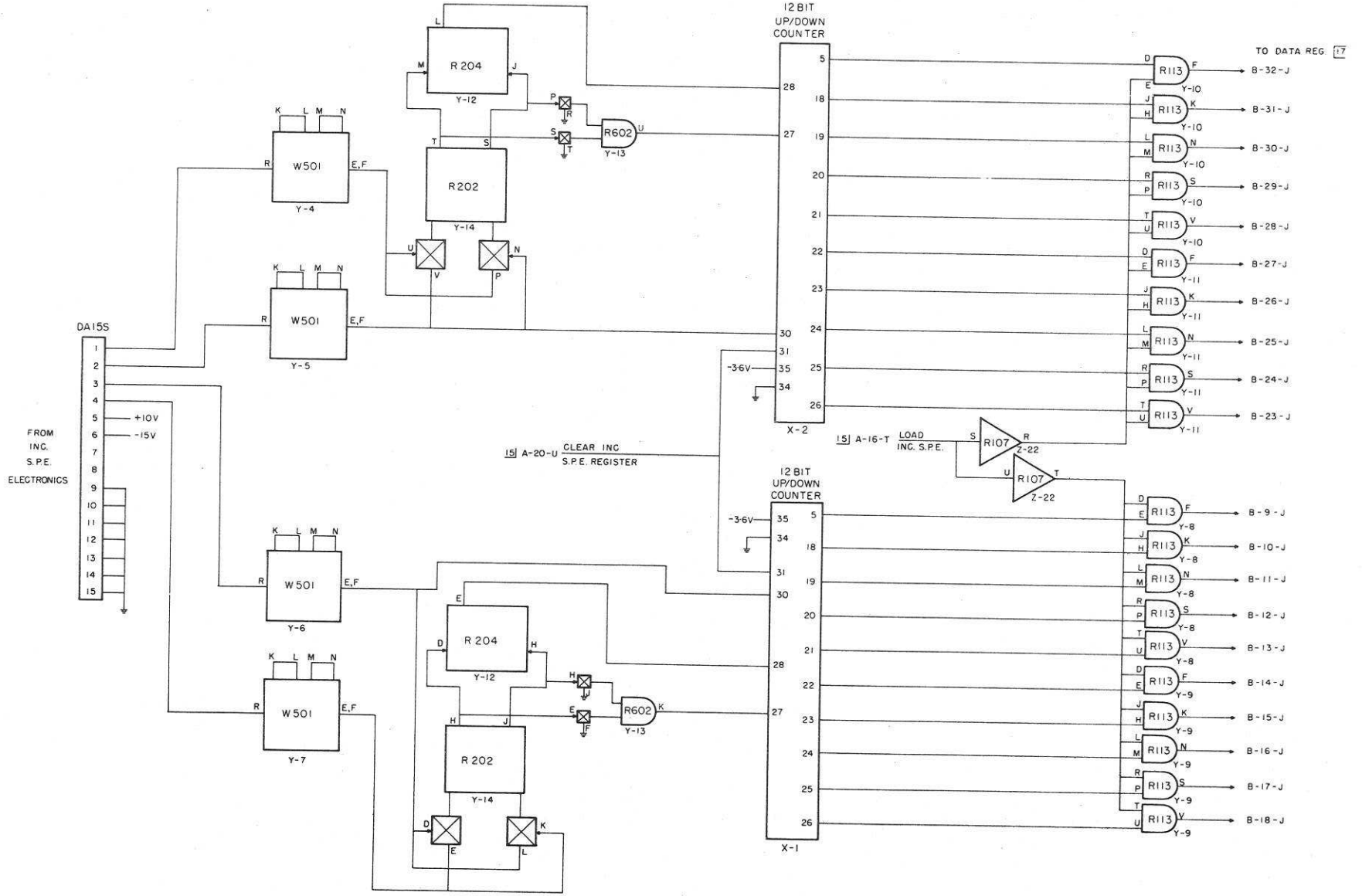


BIT	FROM [17]	INPUT	OUTPUT	D/A CONVERTER CONNECTORS	
0	B-21-M	Z-24-E	Z-24-D	1	
1	B-32-M	Z-24-H	Z-24-F	2	
2	B-31-M	Z-24-K	Z-24-J	3	
3	B-30-M	Z-24-M	Z-24-L	4	
4	B-29-M	Z-24-P	Z-24-N	5	
5	B-28-M	Z-24-S	Z-24-R	6	
6	B-27-M	Z-24-U	Z-24-T	7	0-11 D/A CONVERTER
7	B-26-M	Z-23-E	Z-23-D	8	
8	B-25-M	Z-23-H	Z-23-F	9	
9	B-24-M	Z-23-K	Z-23-J	10	
10	B-23-M	Z-23-M	Z-23-L	11	
11	B-22-M	Z-23-P	Z-23-N	12	
GND				15	
LOAD STROBE	B-4-K			13	
12	B-20-M	Z-23-S	Z-23-R	1	
13	B-9-M	Z-21-U	Z-21-T	2	
14	B-10-M	Z-21-S	Z-21-R	3	
15	B-11-M	Z-21-P	Z-21-N	4	
16	B-12-M	Z-21-M	Z-21-L	5	
17	B-13-M	Z-21-K	Z-21-J	6	
18	B-14-M	Z-21-H	Z-21-F	7	
19	B-15-M	Z-21-E	Z-21-D	8	12-23 D/A CONVERTER
20	B-16-M	Z-22-E	Z-22-D	9	
20	B-17-M	Z-22-H	Z-22-F	10	
22	B-18-M	Z-22-K	Z-22-J	11	
23	B-19-M	Z-22-M	Z-22-L	12	
GND				15	
LOAD STROBE	B-4-K			13	

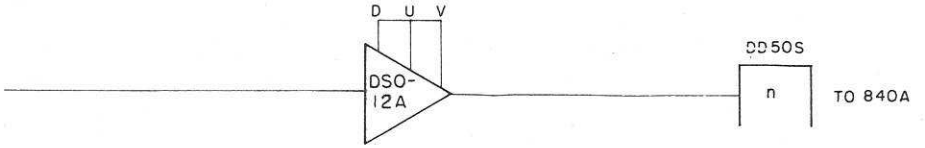
Drawing No. DS-1-34D. Data register D/A converter



Drawing No. DS-1-37D. Event counter

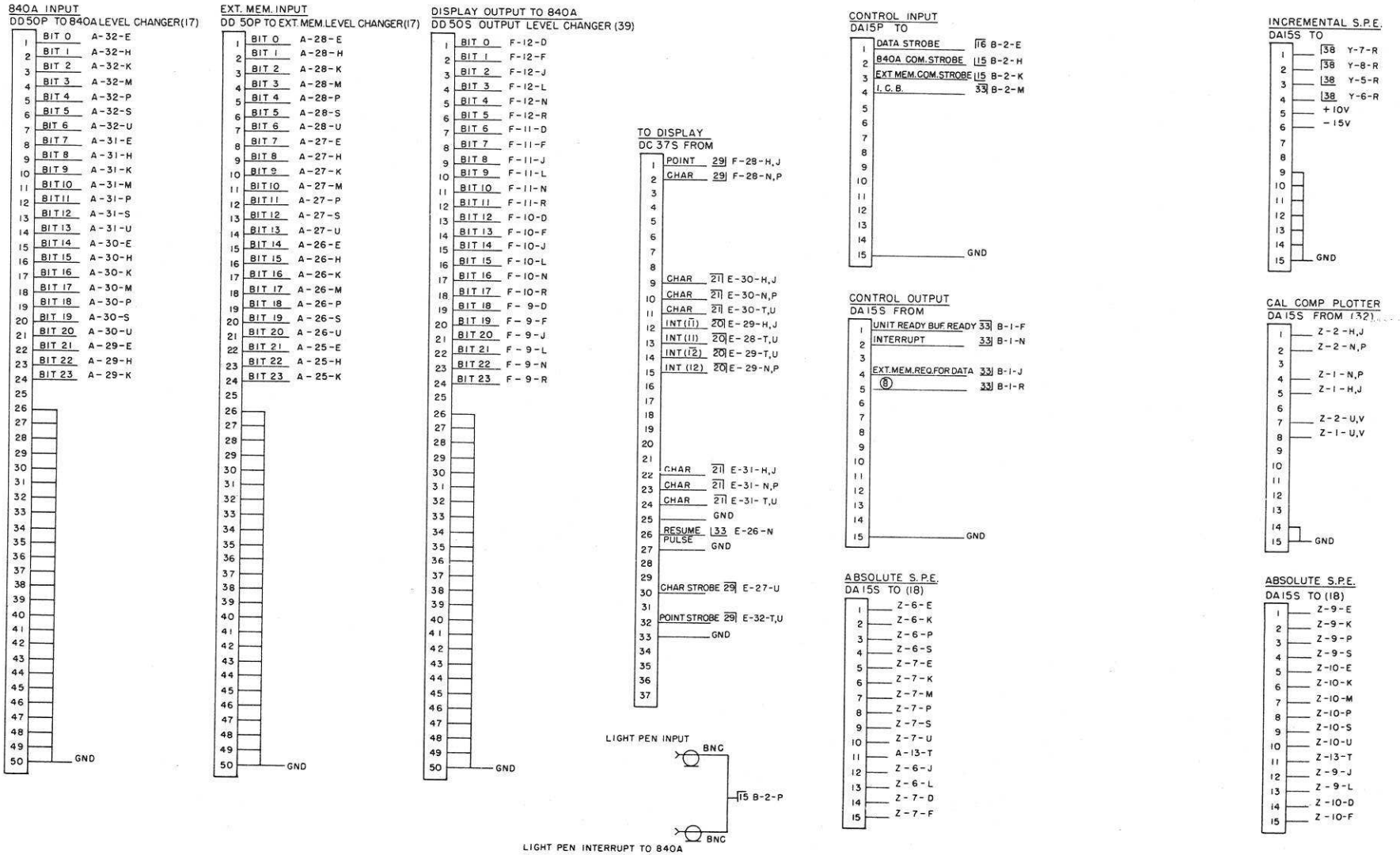


Drawing No. DS-1-38D. Incremental shaft position encoder

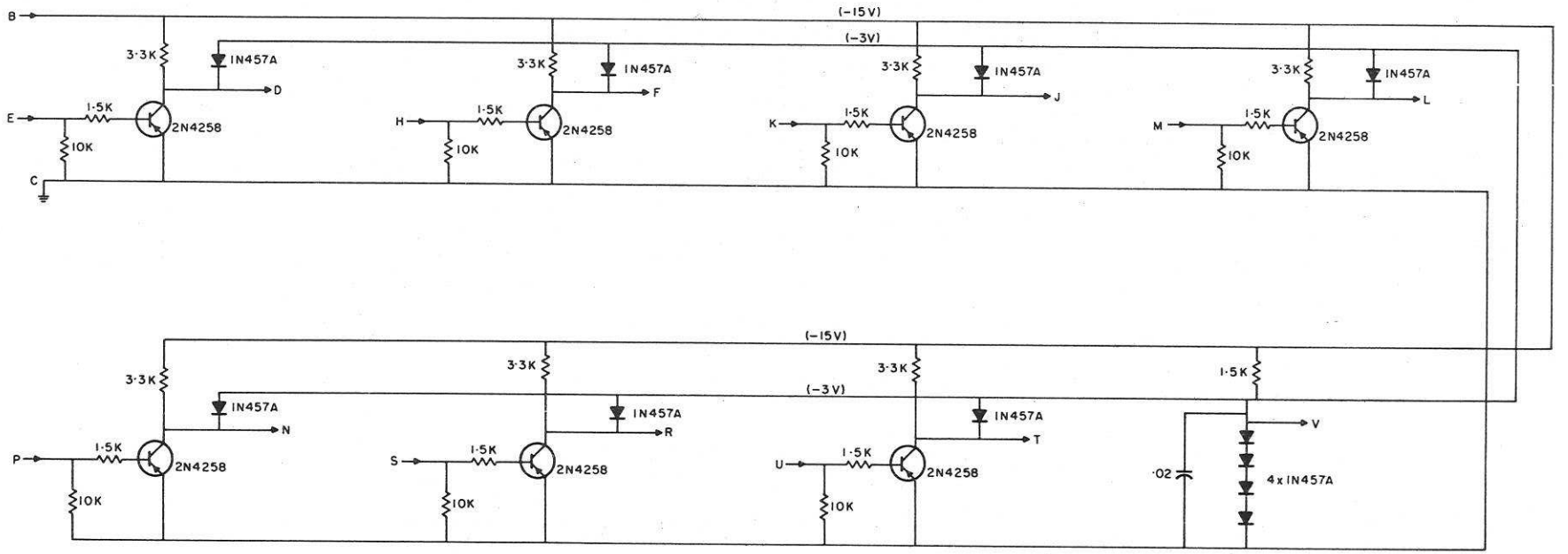


BIT	INPUT FROM DATA REG. (17)	INPUT	OUTPUT	CONNECTOR PIN NO.
0	B-21-M	F-12-E	F-12-D	1
1	B-32-M	F-12-H	F-12-F	2
2	B-31-M	F-12-K	F-12-J	3
3	B-30-M	F-12-M	F-12-L	4
4	B-29-M	F-12-P	F-12-N	5
5	B-28-M	F-12-S	F-12-R	6
6	B-27-M	F-11-E	F-11-D	7
7	B-26-M	F-11-H	F-11-F	8
8	B-25-M	F-11-K	F-11-J	9
9	B-24-M	F-11-M	F-11-L	10
10	B-23-M	F-11-P	F-11-N	11
11	B-22-M	F-11-S	F-11-R	12
12	B-20-M	F-10-E	F-10-D	13
13	B-9-M	F-10-H	F-10-F	14
14	B-10-M	F-10-K	F-10-J	15
15	B-11-M	F-10-M	F-10-L	16
16	B-12-M	F-10-P	F-10-N	17
17	B-13-M	F-10-S	F-10-R	18
18	B-14-M	F-9-E	F-9-D	19
19	B-15-M	F-9-H	F-9-F	20
20	B-16-M	F-9-K	F-9-J	21
21	B-17-M	F-9-M	F-9-L	22
22	B-18-M	F-9-P	F-9-N	23
23	B-19-M	F-9-S	F-9-R	24

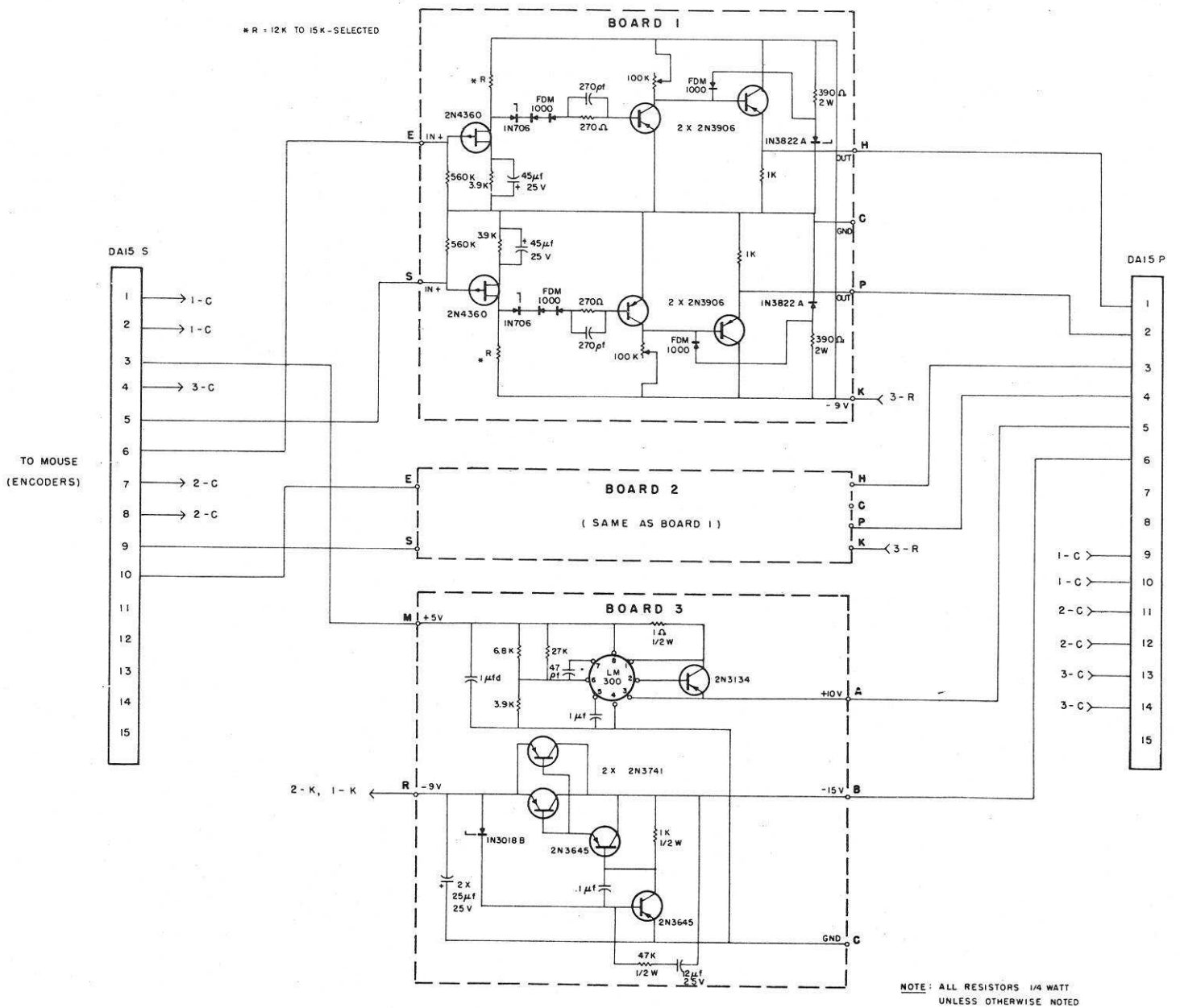
Drawing No. DS-1-39D. Output level changers



Drawing No. DS-1-40D. Connectors



Drawing No. DS-1-42D. Shaft position encoder (S.P.E.) inverters



Drawing No. DS-1-46D. Incremental shaft position encoder amplifiers