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INSTRUCTIONS FOR
SWEEP DELAY UNIT NO. 74A (A.A. NO. 4 MK. 6/1)

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ORIGINAL SIGNED BY
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J.Y. Wong
1985

OTTAWA

NOVEMBER 1951

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~~SECRET~~INSTRUCTIONS FOR SWEEP DELAY UNIT No. 74A (A.A.No.4 Mk.6/1)GENERAL DESCRIPTION

The maximum range that can be displayed with the present sweep is 120,000 yards. By the addition of Sweep Delay Unit No. 74A the maximum displayable range may be increased by approximately 40,000 to 100,000 yards. This is accomplished by delaying the initiation of the sweep for a predetermined time interval after the transmitter pulse. This delay can be calibrated by reference to the calibration rings on the PPI. Unit No. 74A may be switched in or out of the circuit, as desired.

INSTRUCTIONS FOR SWEEP DELAY UNIT No. 74A (A.A.No.4 Mk.6/1)DETAILED TECHNICAL DESCRIPTIONACTION OF DELAY CHASSIS SWITCH

(see Figs. 1 and 2)

- Position (1) **NORMAL** The input trigger is bypassed through the delay chassis to give normal instantaneous sweep triggering with the B+ for the blocking "oscillator" switched off.
- Position (2) **DELAY** The input trigger from the modulator is delayed by using it to trigger a phantastron. The trailing edge of its output triggers a blocking pulse generator whose output pulse starts the sweep on the PPI.
- Position (3) **CAL.** Both the delay chassis and the sweeps are triggered together by the modulator pulse. The delayed pulse so derived is coupled into the video via the plate of V_{15} in chassis No. 74. The new "range ring" produced can be brought into coincidence with any 10,000 yard range ring so that on DELAY, the range indicated has this present range added to give the actual range of a target.

INSTRUCTIONS FOR SWEEP DELAY UNIT No. 74A (A.A.No.4 Mk.6/1)

ACTION (see Figs. 1 and 2)

Phantastron V_{14} , V_{15} , V_2

I

GENERAL DESCRIPTION

The maximum range that can be displayed with the present sweep is 120,000 yards. By the addition of Sweep Delay Unit No. 74A the maximum displayable range may be increased by approximately 40,000 to 100,000 yards. This is accomplished by delaying the initiation of the sweep for a predetermined time interval after the transmitter pulse. This delay can be calibrated by reference to the calibration rings on the PPI. Unit No. 74A may be switched in or out of the circuit, as desired.

II

DETAILED TECHNICAL DESCRIPTION

ACTION OF DELAY CHASSIS SWITCH

(see Figs. 1 and 2)

- Position (1) **NORMAL** The input trigger is bypassed through the delay chassis to give normal instantaneous sweep triggering with the B+ for the blocking "oscillator" switched off.
- Position (2) **DELAY** The input trigger from the modulator is delayed by using it to trigger a phantastron. The trailing edge of its output triggers a blocking pulse generator whose output pulse starts the sweep on the PPI.
- Position (3) **CAL.** Both the delay chassis and the sweeps are triggered together by the modulator pulse. The delayed pulse so derived is coupled into the video via the plate of V_{15} in chassis No. 74. The new "range ring" produced can be brought into coincidence with any 10,000 yard range ring so that on DELAY, the range indicated has this present range added to give the actual range of a target.

CIRCUIT ACTION (see Figs. 3 and 4)

Phantastron V_{1A} , V_{1B} , V_2

In the quiescent state, the screen of V_2 is conducting heavily and no current flows in the plate circuit by virtue of suppressor cut-off. On application of a negative trigger via diode V_{1A} to the plate of V_2 , the plate drops, and, with it, grid No.1 drops by coupling through C_1 , reducing the current to the screen. The sudden reduction in screen current in the resistor R_2 causes the suppressor to rise via R_3 , R_4 , and speed-up condenser C_2 . This action allows the plate to conduct. Note that the plate and grid of V_2 are coupled by C_1 , R_1 , so that the plate-fall rate is limited by the discharge of C_1 through R_1 and by the rate of change of potential between the grid and plate. Thus the plate falls with an effective time constant $R_1 C_1 (1 + A)$ where A = amplification factor of V_2 . When the plate bottoms, the screen current increases causing the screen voltage to fall. This fall is coupled to the suppressor, cutting off plate current, and the plate rises through time constant $C_1 R_1$. Diode V_{1A} is used to terminate the plate rise, and hence to give delay control.

Since the cathode resistor, R_C , of V_2 conducts plate current, then screen current, a change from low plate current to high screen current causes a sharp rise in cathode voltage and vice versa.

The rising edge of the cathode rectangular wave is differentiated and used to trigger the blocking pulse generator.

Blocking Pulse Generator V_{3A} , V_{3B}

The cathodes and plates of V_{3A} and V_{3B} are coupled together, the cathode voltage being such that both tubes are cut off. The application of a positive trigger to the grid of V_{3A} causes the plates of V_{3A} and V_{3B} to fall. The grid and plate windings of transformer, T , are connected antiphase so that the plate fall in V_{3B} causes a sharp grid rise. The positive feedback causes V_{3B} to conduct heavily, and to discharge C_3 . This action causes a sharp negative going pulse to be generated on the plate of V_{3B} . When the plate fall ceases, the plate rises sharply causing the grid voltage to go rapidly negative. (With no output loading, the plate voltage will overshoot.) Since C_3 has been discharged,

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the pulse generator cannot be retriggered until C_3 is charged through R_8 ($R_8 = R_5 + R_6$). The termination of the output coil of T by R_{26} in chassis No. 74 eliminates the positive overshoot in the output pulse.

Waveforms

See Fig. 4.

Bringing the Equipment into Action (see Fig. 5)

Set Switch 1, Unit 74A, to "calibrate". An extra ring should appear on the PPI tube. This ring can be moved in and out in range by turning potentiometer P_1 , Unit 74A.

Set the delay ring to coincide with the range ring corresponding to the desired delay.

Operating the Delay Unit

To operate Unit 74A, set switch to "delay" and add the delay to the range read on the tube.

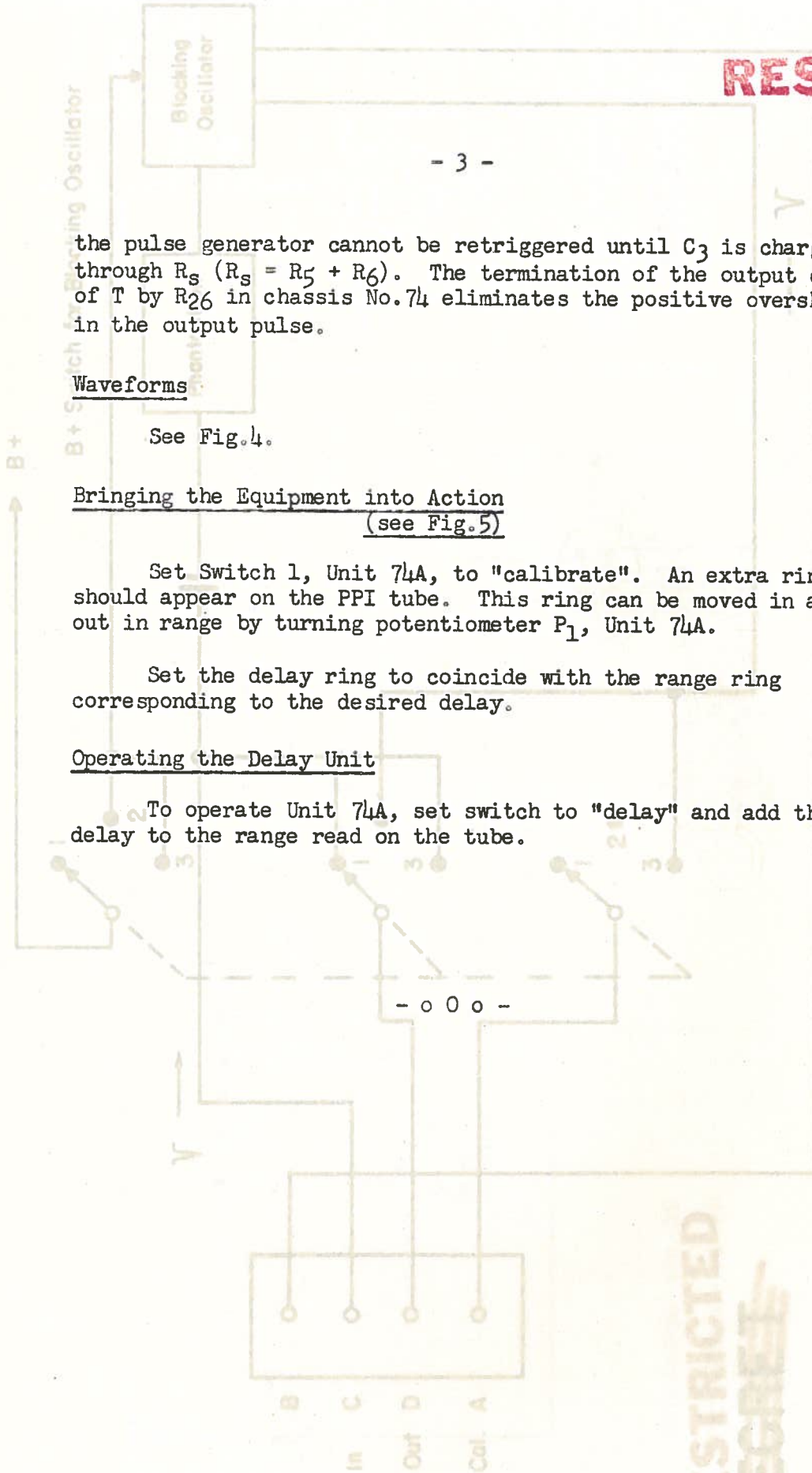


Fig. 1 SWITCHING SCHEMATIC

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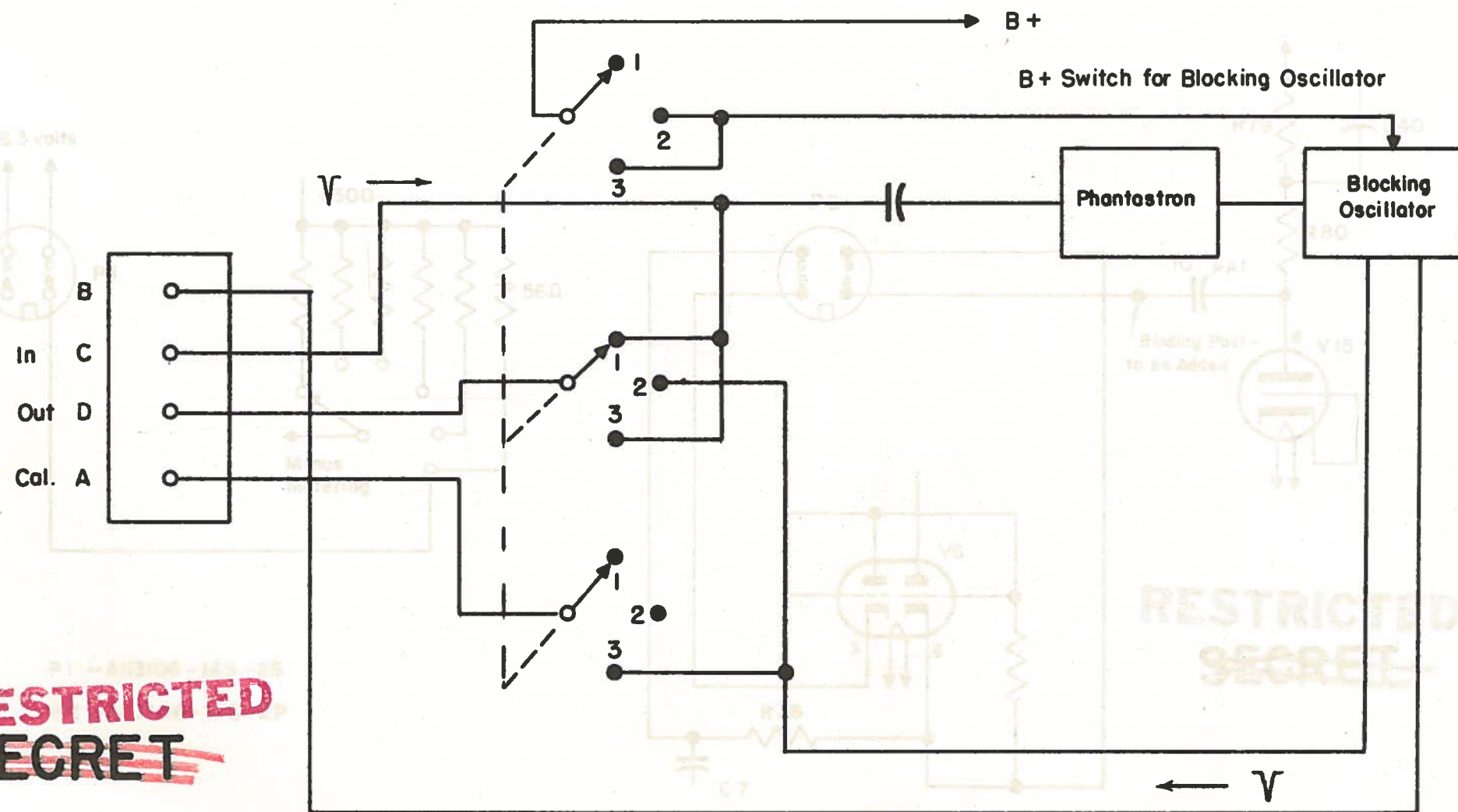
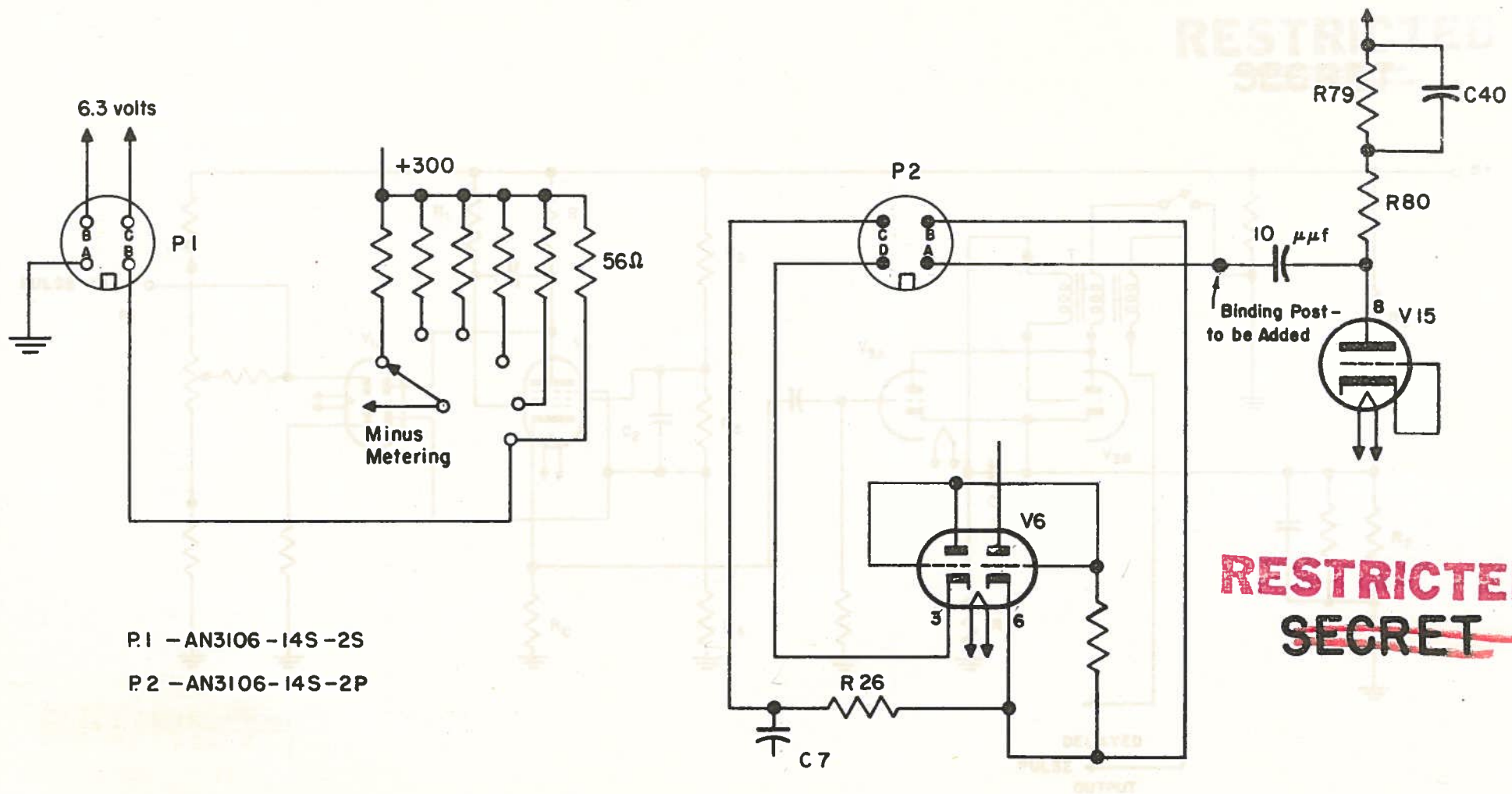


Fig. 2 CONNECTIONS TO UNIT 74

Fig. 1 SWITCHING SCHEMATIC



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Fig. 2 CONNECTIONS TO UNIT 74

Fig. 3 SIMPLIFIED SCHEMATIC OF SWEEP DELAY CIRCUIT

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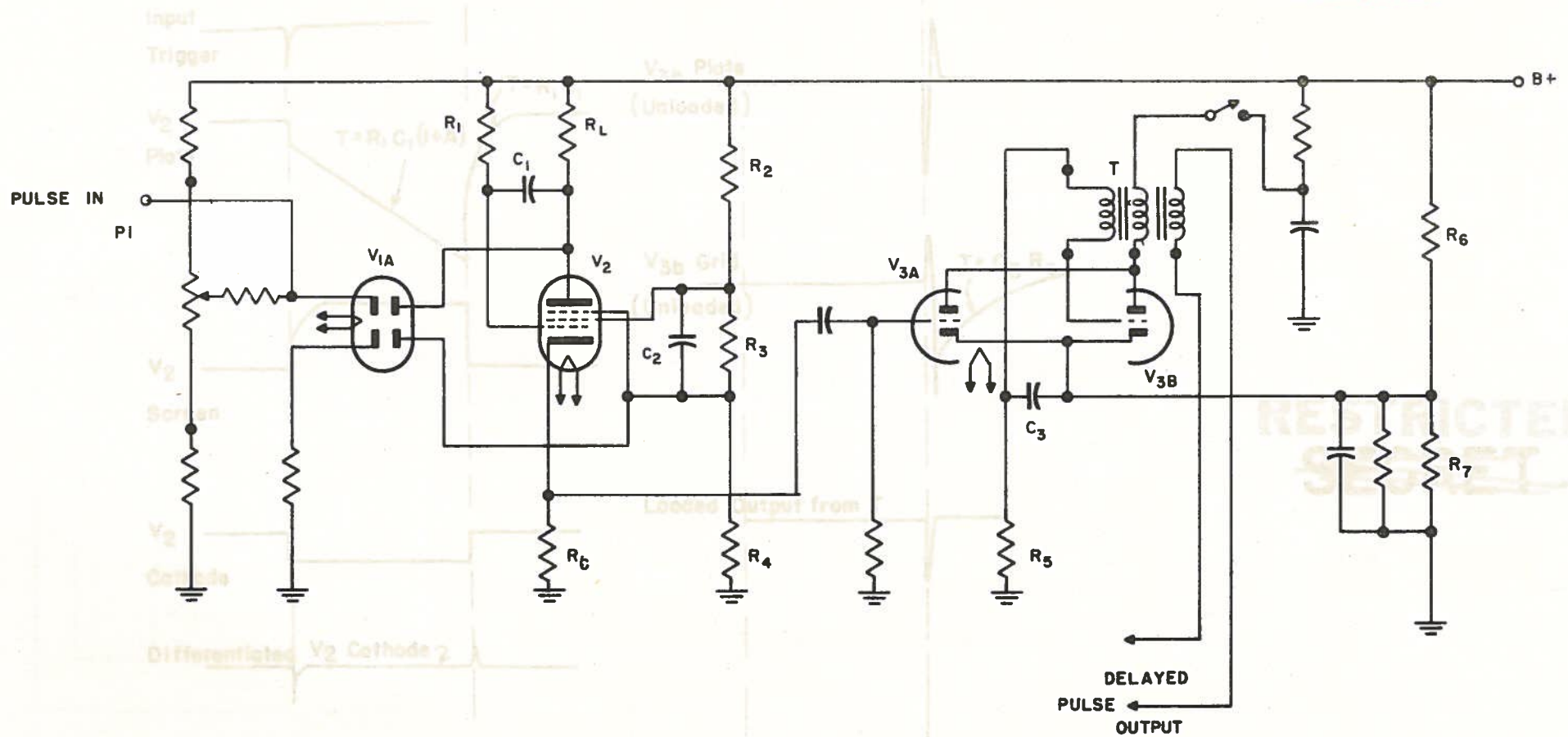
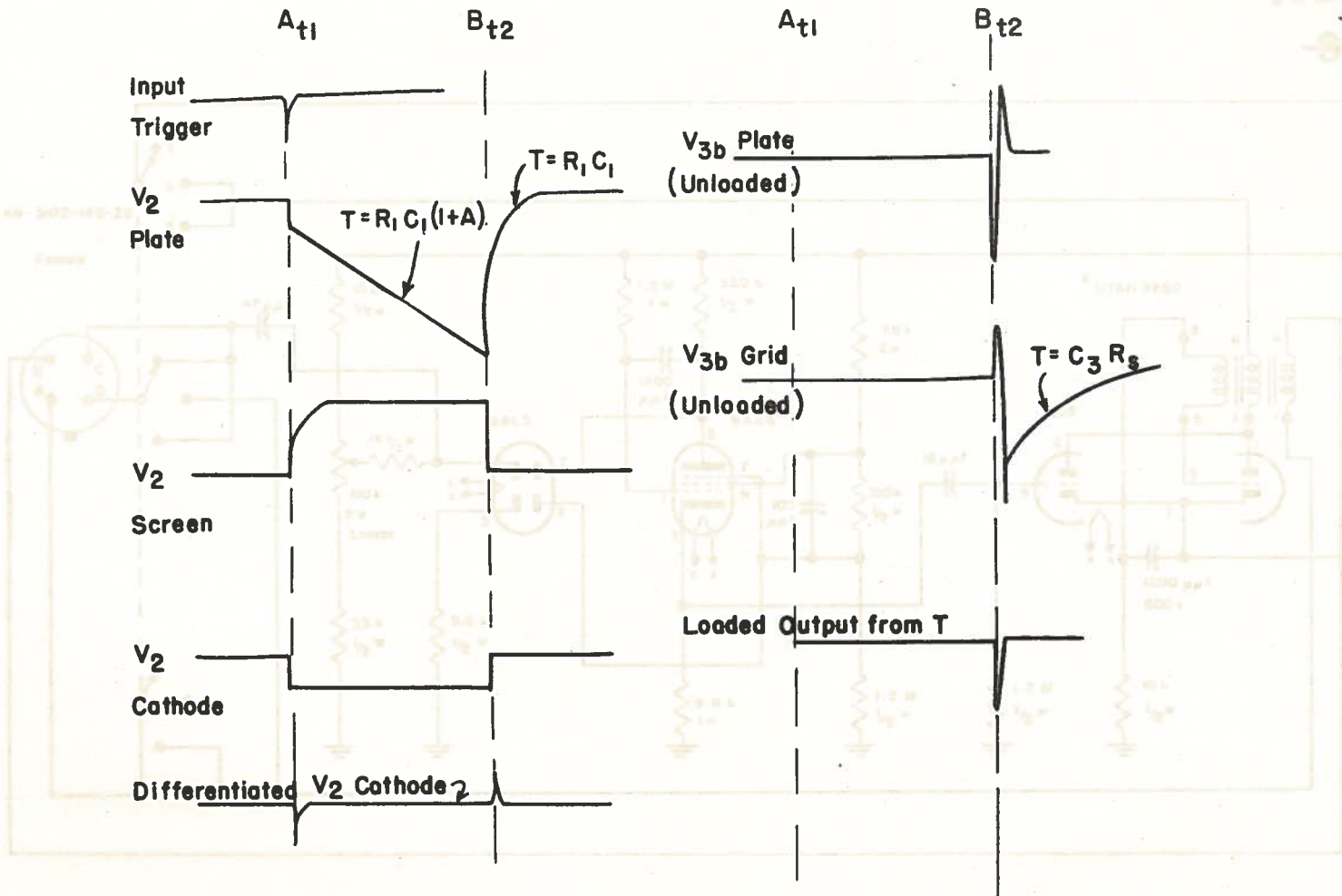


Fig. 3 SIMPLIFIED SCHEMATIC OF SWEEP DELAY CIRCUIT

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Fig. 4 WAVEFORMS — SWEEP DELAY CIRCUIT

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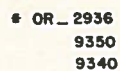


Fig. 5 A. A. No.4 MK. 6/1 - SWEEP DELAY CIRCUIT UNIT 74A