The development of an integrated circuit data encoder for a particle-counting satellite experiment

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THE DEVELOPMENT OF AN INTEGRATED CIRCUIT DATA ENCODER FOR A PARTICLE-COUNTING SATELLITE EXPERIMENT

- T. H. SHEPERTYCKI -

OTTAWA

JANUARY 1969

ABSTRACT

This report describes the development of a sixteen-channel integrated-circuit data encoder that is part of a particle-counting experiment in the ISIS-A satellite. Emphasis is placed on the design factors which affect the reliability and performance of the encoder. An attempt is made to give the prospective experimenter a feel for the meticulous attention to detail that is necessary in the design, construction, and testing of spacecraft equipment. Some of the constraints that are beyond the control of the experimenter are discussed.

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– T.H. Shepertycki –

Introduction

The ISIS-A satellite (International Satellite for Ionospheric Studies) is the third scientific satellite designed and constructed in Canada as part of a joint Canada–USA program aimed at orbiting instruments designed to make the measurements required for study of many important ionospheric phenomena [1].

One of the experiments conducted with this spacecraft is an energetic-particle-detection (EPD) experiment devised by the Division of Pure Physics of the National Research Council. The primary purpose of this experiment is to measure the angular distributions and energy spectra of electrons ranging from 20 keV to greater than 2.8 MeV and of protons ranging from 150 keV to greater than 45 MeV. Two packages (Plate I) contain the required instrumentation: a detector package designed by the Cosmic Ray Section of the Pure Physics Division, and a data encoder package designed by the Data Systems Section of the Radio and Electrical Engineering Division [2, 3]. This report describes the design, construction, and testing of three models of the data encoder – one engineering and two flight models. Our undertaking in this program was begun in the spring of 1964 and construction was successfully completed in the spring of 1968. The ISIS-A satellite is scheduled for launching in January 1969.

System Description

Electron and proton detection is accomplished in the detector package located at the skin of the satellite. The pulses from eleven particle detectors in this package are amplified and passed through amplitude discriminators prior to entering the encoder package for further data processing.

The encoder, Fig. 1(*a*), is designed to perform several functions: first, to count these pulses over time periods of $\frac{1}{4}$ second; second, to provide directional information by digitizing the outputs of four magnetometers; third, to monitor the occurrence of several single-bit events such as will be discussed later. Finally, on command from the satellite's PCM encoder, these data are read out in a manner conducive to relatively simple data processing on the ground.

A block diagram of the encoder, Fig. 1(*b*), shows sixteen binary counters, a 16-position word commutator, a 16-position bit commutator, a 6-channel analog multiplexer, an 8-bit analog-to-digital converter, a frame sync pattern generator, a parity generator, and input–output interfaces.

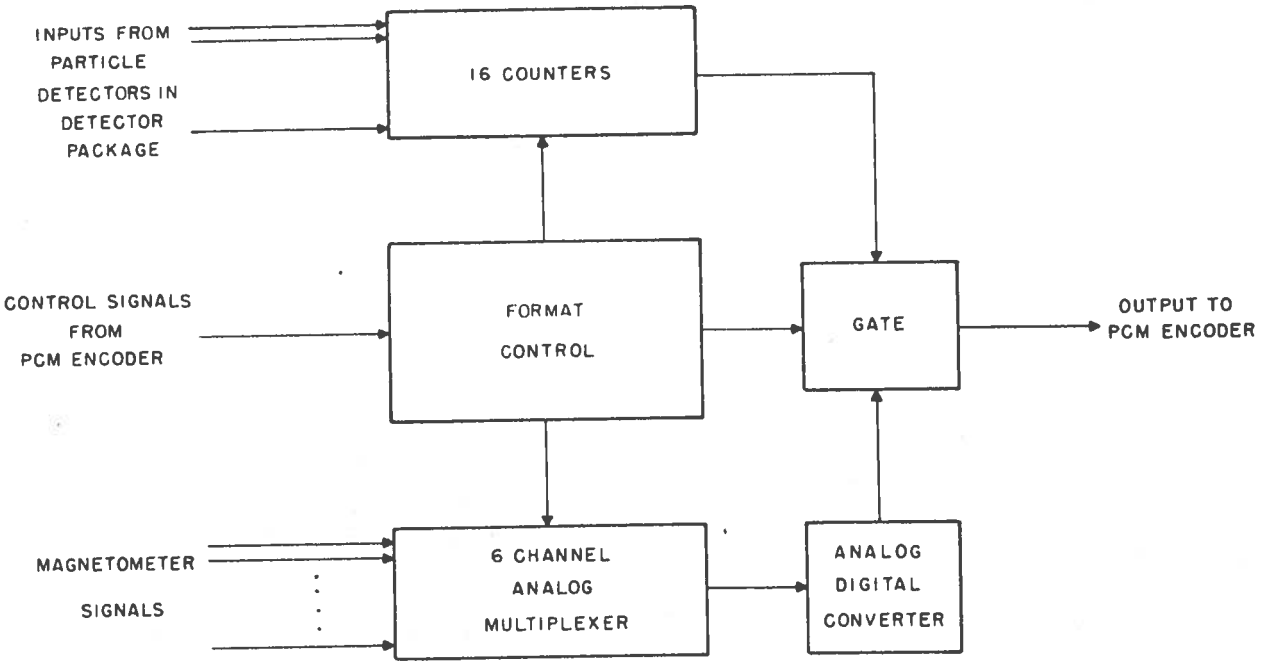


Figure 1(a) Functional diagram of encoder

The manner in which the data are organized is shown in Fig. 2. One frame of data consists of sixteen 16-bit words. The beginning of each frame is marked by a fixed frame synchronization pattern labeled word 1. The remaining words, with the exception of word 10, represent the outputs of either 2^{15} counters, like words 2, 5, 6, 7, etc.; or 2^{13} counters, like words 3, 4, and 8; or 2^{7} and 2^{8} counters, like words 15 and 16. The most significant bit of each word appears at the left of each word in bit 1 position, with the least significant bit appearing in the 15th-bit position. The odd parity bit generated for words 2 to 16 makes the frame synchronization pattern in word 1 unique, since it was chosen to have even parity.

The seven bits marked *A* to *G* in bit positions 9 to 15 of word 10 are flag bits which monitor events. For example, the encoder package provides a switching signal every alternate frame to the detector package, which is used to control the bias levels on the amplitude discriminators associated with the particle detectors whose outputs are represented by words 5 and 6. If, in one frame, words 5 and 6 represent electron counts $>$ 40 keV and 80 keV, respectively, then in the following frame they will represent electron counts $>$ 60 keV and 100 keV, respectively. The state of this switching signal is monitored by flag bit *G*.

Flag bit *A* records the time at which a low-level current amplifier in the 20 keV photomultiplier detector in the detector package is being calibrated.

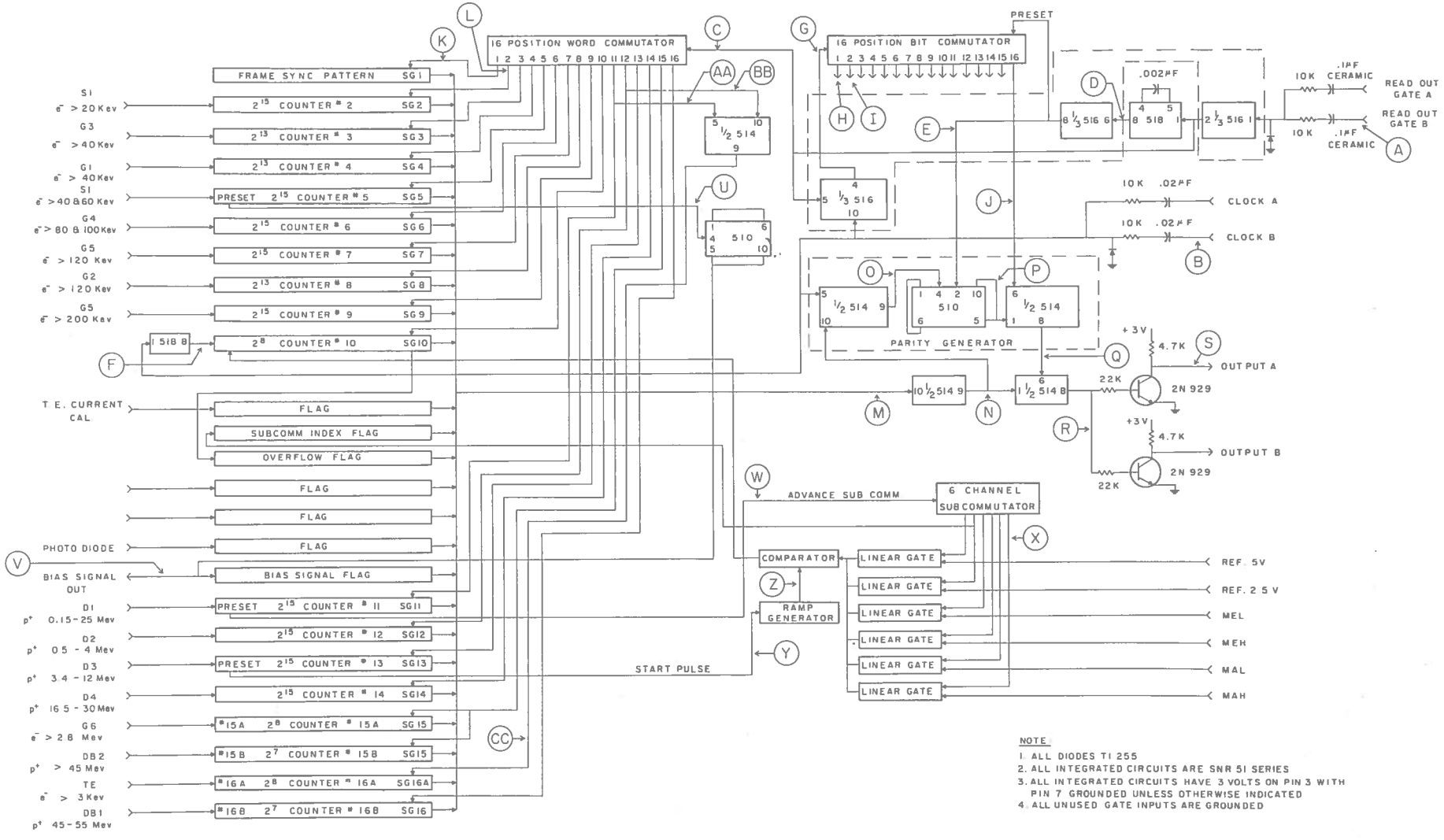


Figure 1(b) Block diagram of encoder

WORD No.	MSB 1	2	3	4	5	6	7	8	BIT No. 9	10	11	12	13	14	15	LSB 16
1	0	0	0	1	0	1	0	0	0	1	1	0	1	1	1	1
2	2^{15} COUNTER ; S_1 PHOTOMULTIPLIER e^- > 20 Kev															P
3	0	0	2^{13} COUNTER ; G_3 GEIGER e^- > 40 Kev													P
4	0	0	2^{13} COUNTER ; G_1 GEIGER e^- > 40 Kev													P
5	2^{15} COUNTER ; S_1 PHOTOMULTIPLIER e^- > 40 & 60 Kev SWITCHED ON ALT. FRAMES															P
6	2^{15} COUNTER ; G_4 GEIGER e^- > 80 & 100 Kev SWITCHED ON ALT. FRAMES															P
7	2^{15} COUNTER ; G_5 SiJ e^- > 120 Kev															P
8	0	0	2^{13} COUNTER ; G_2 GEIGER e^- > 120 Kev													P
9	2^{15} COUNTER ; G_5 SiJ e^- > 200 Kev															P
10	MAGNETOMETER & CAL. DATA (8 BITS)								FB A	B	C	D	E	F	G	P
11	2^{15} COUNTER ; D_1 SiJ p^+ 0.15 – 25 Mev															P
12	2^{15} COUNTER ; D_2 SiJ p^+ 0.5 – 4 Mev															P
13	2^{15} COUNTER ; D_3 SiJ p^+ 3.4 – 12 Mev															P
14	2^{15} COUNTER ; D_4 SiJ p^+ 16.5 – 30 Mev															P
15	2^8 COUNTER ; G_6 GEIGER e^- > 2.8 Mev								2^7 COUNTER ; DB_2 SiJ p^+ 45 – 55 Mev							P
16	2^8 COUNTER ; S_1 PHOTOMULTIPLIER e^- > 3 Kev								2^7 COUNTER ; DB_1 SiJ p^+ > 45 Mev							P

FLAG BITS : A - CALIBRATION OF S_1 - 16
B - SUB-COMMUTATOR INDEX
C - OVERFLOW
D - SPARE
E - SPARE
F - STATE OF PHOTO-DIODE
G - STATE OF S_1-5 & G4

Figure 2 Encoder data format

A photomultiplier detector in the detector package is sensitive not only to electrons, but also to radiation in the visible part of the spectrum. Warning of this occurrence is provided by a photo-diode sun sensor, which is mounted in the detector package. When the output from this photo-diode exceeds a certain threshold, this event is recorded by flag bit *F*.

The first eight bits of word 10 represent magnetometer and calibration data. During any one frame, one of six analog voltages is selected, digitized and read out as the first half of word 10. A complete cycle of four magnetometer readings and two calibration readings occurs once every eight frames. Two of the four magnetometers are sampled twice as often as the other two. To achieve subcommutator synchronization on the ground, flag bit *B* records a *one* whenever the 2.5-volt reference signal appears in the first half of word 10. Flag bit *C* is an overflow indicator for counter No. 10 which forms part of the analog-to-digital converter. This is necessary when the magnetometer voltages, normally 0 to 5 volts, increase to 6 volts as happens in certain instances.

Flag bits *D* and *E* are spares and show up in the output as *zeros*. If extra flag bits were required, they could be inserted in bit positions 1 and 2 of words 3, 4, and 8.

Electrical Design

The primary design criteria for satellite-borne equipment are reliability, low weight, and low power consumption. In the development of the encoder these three factors were best satisfied by the use of silicon integrated circuits and, in particular, by the relatively low-power resistor-capacitor-transistor-logic (RCTL) circuits, Series 51, manufactured by Texas Instruments Ltd. These circuits were capable of handling the maximum frequency present in the encoder, 100 kHz, at a power consumption of 2–3 mW per gate or flip-flop. The availability of these circuits in the small flat TO-87 and 89 package ($\frac{1}{4}$ inch $\times \frac{1}{8}$ inch $\times \frac{1}{32}$ inch) was consistent with the minimal weight requirement. The reliability of these components was supported by the fact that several packages using these circuits had successfully flown in previous satellites.

A detailed description of the functional operation of the encoder (Fig. 1(*b*)) will be given, followed by a discussion of the design factors of the various subsystems. Each of the 16 binary counters is provided with input and output gates and clearing facilities. The operation of these gates is controlled by a word commutator which is, in turn, controlled by a 60-Hz read signal from the satellite's PCM encoder. The counters are allowed to accumulate pulses from their various detectors for $\frac{1}{4}$-sec time periods. The data so stored in the encoder are read out sequentially by the bit commutator stepping at a bit rate of 11.52 kHz as 16 words, each containing 16 bits, with each word separated from the preceding word by $\frac{1}{60}$ sec. Each 16-bit word is read out in 1.39 msec and one complete frame of data is read out in $\frac{4}{15}$ sec. During the sixteenth bit in each word the counter or counters that have just been read out are reset to zero, with the parity generator supplementing the 15 bits with a sixteenth odd parity bit.

An 8-position subcommutator selects one of six analog voltages every frame, for comparison with the output of a linear ramp generator. The output of the comparator controls the number of clock pulses fed into a 2^8 counter. This accumulated count is then proportional to the analog voltage appearing at the input to the comparator, and is interlaced with the output data, as described previously.

Details of the system timing can be obtained from Figs. 3(*a*) and (*b*) which show the timing waveforms at the points in the encoder alphabetically designated in Fig. 1(*b*).

The following sections will discuss in some detail the design factors of the various subsystems comprising the encoder.

a) Input-Output Interface

Encoder timing is derived from word (read-out-gate, ROG) and bit (clock, CLK) synchronization signals received from one of two PCM encoders in the satellite. Only one PCM encoder is active; the other is a back-up.

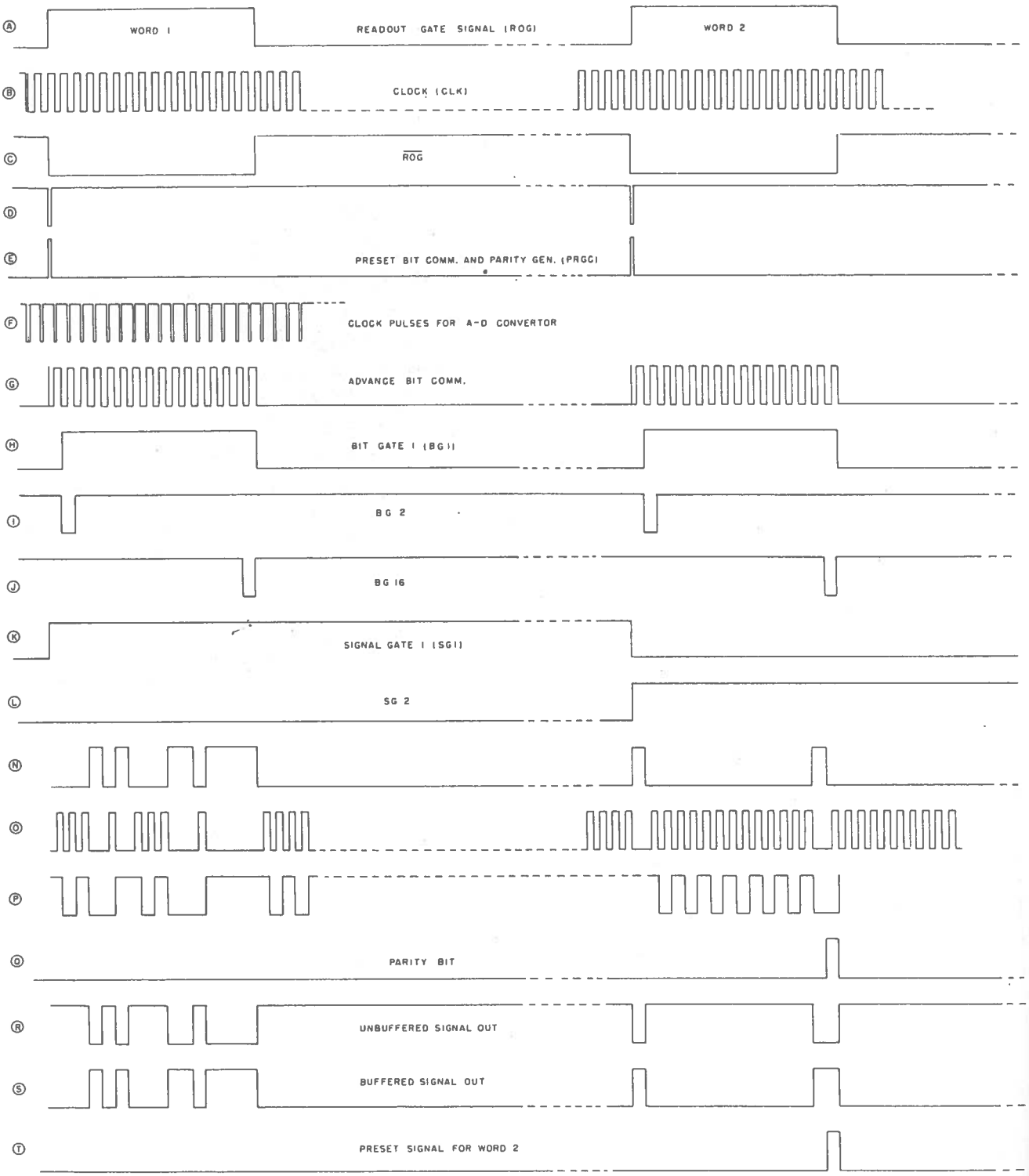


Figure 3(a) Timing diagram

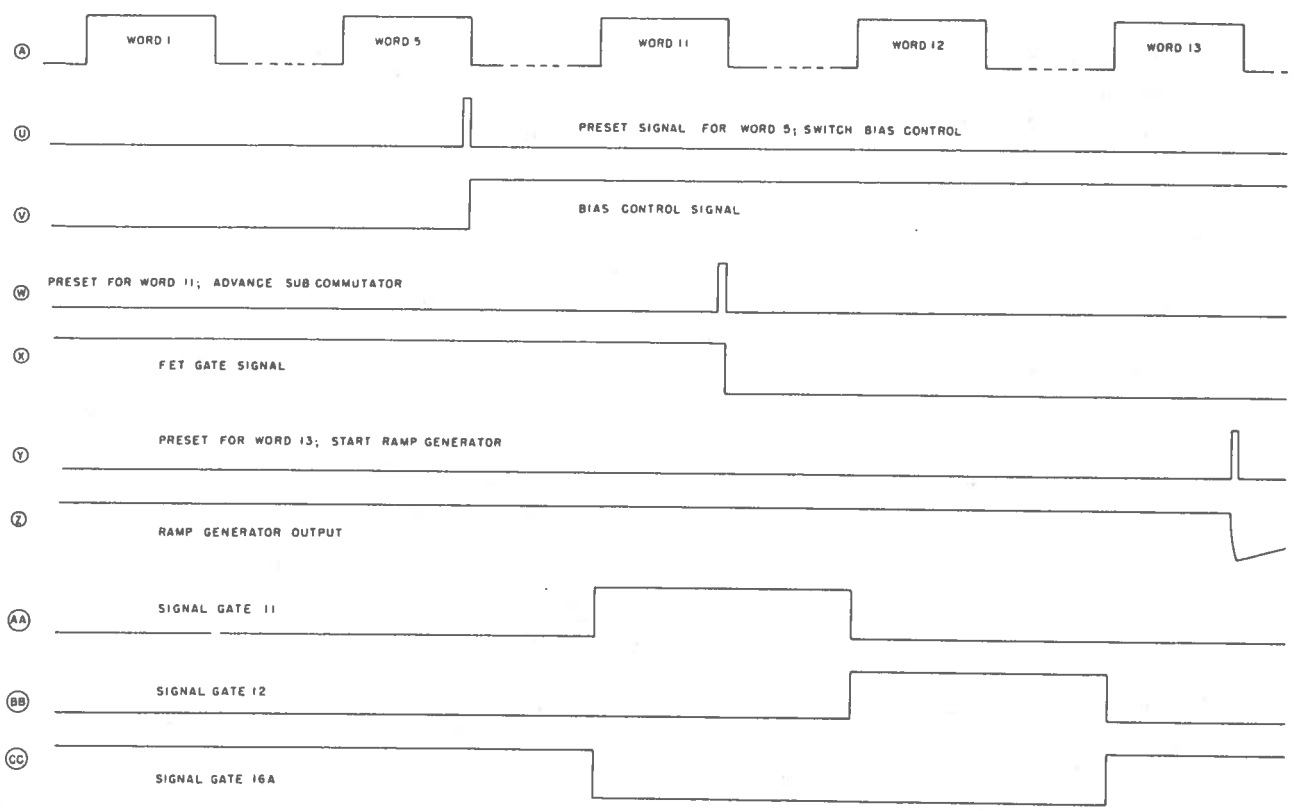


Figure 3(b) Multi-word timing diagram

The input/output signal specifications are as follows:

INPUT CONTROL SIGNALS TO EPD DATA ENCODER

The following specifications apply to both the bit and word synchronization signals.

Amplitude	+6 V minimum	+10 V maximum
Source resistance	1000 Ω maximum	
Rise and fall times < 1 μsec		
Typical load 10 kΩ in parallel with 200 pF		
Fault voltage ± 20 V from a source resistance of 10 kΩ		

BIT SYNC RATE

Square wave output at the bit rate (11,520 pps nominal) with a 'Mark' to 'Space' ratio of 1±0.1.

WORD SYNC RATE

At frame rate	60 pps
Duration	1392 μsec nominal ± 2%

In addition the maximum relative delay between the half amplitude point of the positive going edge of the word sync output and the half amplitude point of the positive going edge of the bit sync output shall be less than ± 1 μsec.

The input interface problem was solved by the simple resistor-capacitor-diode networks shown in Fig. 1(*b*).

OUTPUT SIGNAL FROM EPD DATA ENCODER

The binary information from the EPD data encoder must be represented by the following voltage levels:

'1' level voltage	+2.0 to +2.5 V
'0' level voltage	0.0 to +0.5 V
Source resistance	< 5000 Ω
Rise and fall times	< 5 μsec

In addition the leading edge of the most significant bit of the output word from the EPD data encoder shall be delayed no more than 20 μsec from the leading edge of the word sync signal.

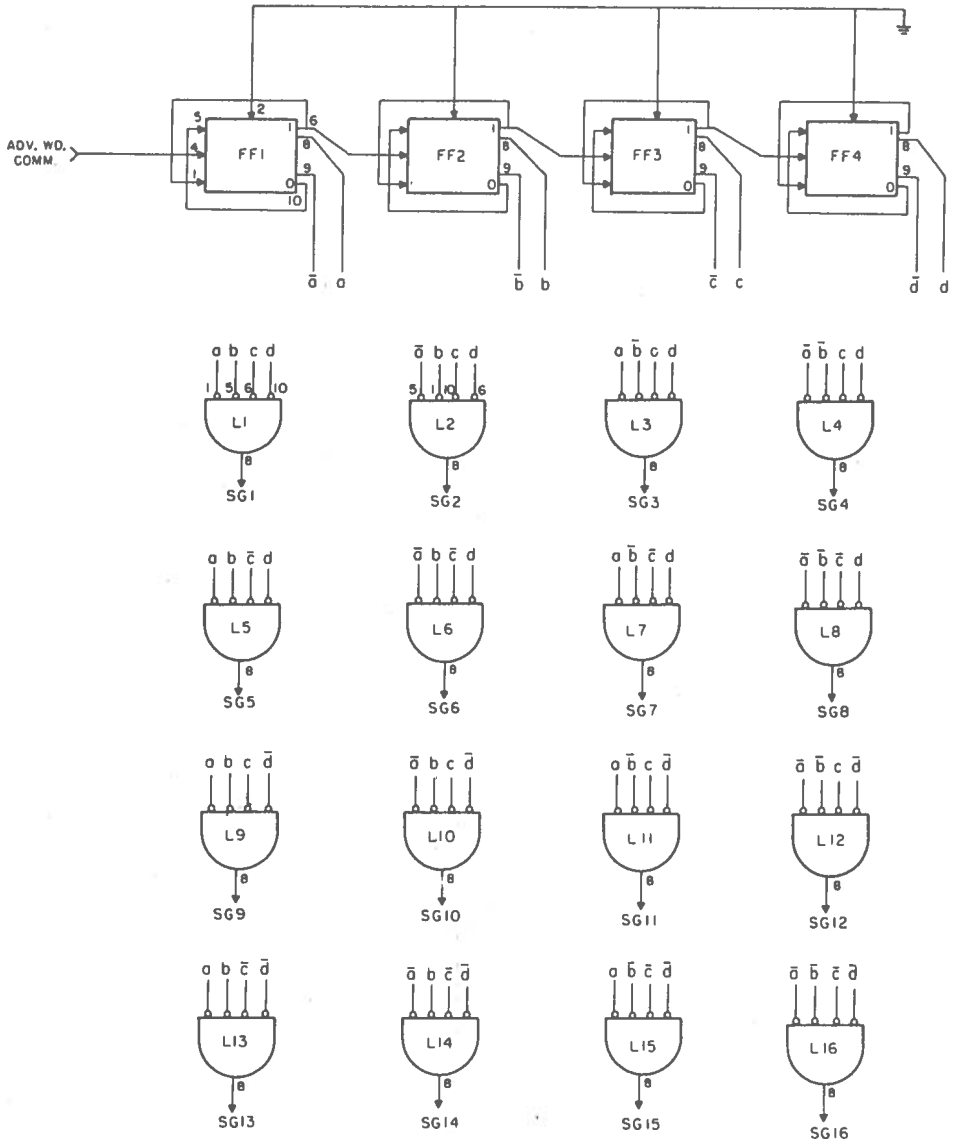
The above conditions are met by delivering the data encoder output to the PCM encoder through the discrete-component common emitter amplifiers shown in Fig. 1(*b*).

b) Word Commutator

The circuit diagram of the word commutator, Fig. 4, consists of a 4-stage binary counter driving a decoding matrix comprising sixteen 4-input NAND gates. The race hazards in this design are non-critical; e.g., at the 2-input signal gate to the counters the decoding spikes appearing on the input gate signal are inhibited by the short information pulses which drop towards ground from a +3-V level.

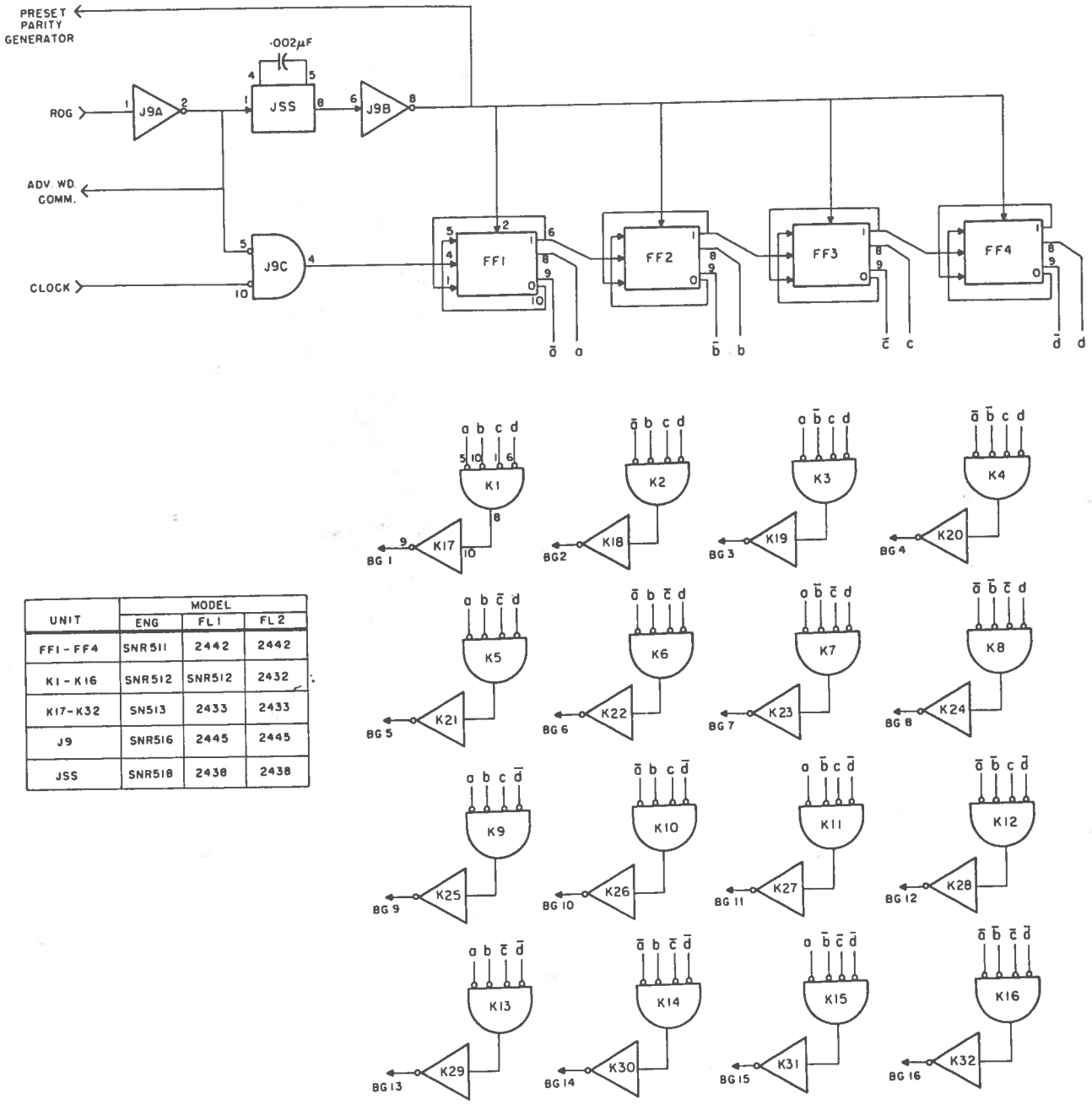
c) Bit Commutator

The circuit diagram of the 16-stage bit commutator is shown in Fig. 5. Like the word commutator is consists of a 4-stage binary counter with a decoding matrix consisting of sixteen 4-input NAND gates. Inverters complement the outputs of these gates. The race hazards in this design are identical with those in the word commutator. Figure 6 shows the 16 outputs from the decoding matrix. Note that decoding spikes appear on the odd-numbered bit gates 1, 3, 5, ... 15. These race hazards are potentially critical for the parity generator and the counter reset circuitry. The manner in which the parity generator is designed to make these race hazards non-critical is described in Section *e*.



	MODEL		
	ENG	FL1	FL2
FF1 – FF4	SNR511	2442	2442
L1 – L16	SNR512	SNR512	2432

Figure 4 Logic diagram of word commutator



UNIT	MODEL		
	ENG	FL 1	FL 2
FF1 - FF4	SNR511	2442	2442
K1 - K16	SNR512	SNR512	2432
K17 - K32	SN513	2433	2433
J9	SNR516	2445	2445
JSS	SNR518	2438	2438

Figure 5 Logic diagram of bit commutator

The pulses which reset the counters to zero after read-out are generated by combining bit-gate 16 with the appropriate word gate. To ensure that the counter is not accidentally reset to zero before read-out has occurred, bit-gate 16 should not contain decoding spikes. Note that timing relationships in Fig. 6 prohibit the presence of decoding spikes in bit gate 16. In addition, the absence of decoding spikes here ensures that decoding spikes on the output gate signals are inhibited.

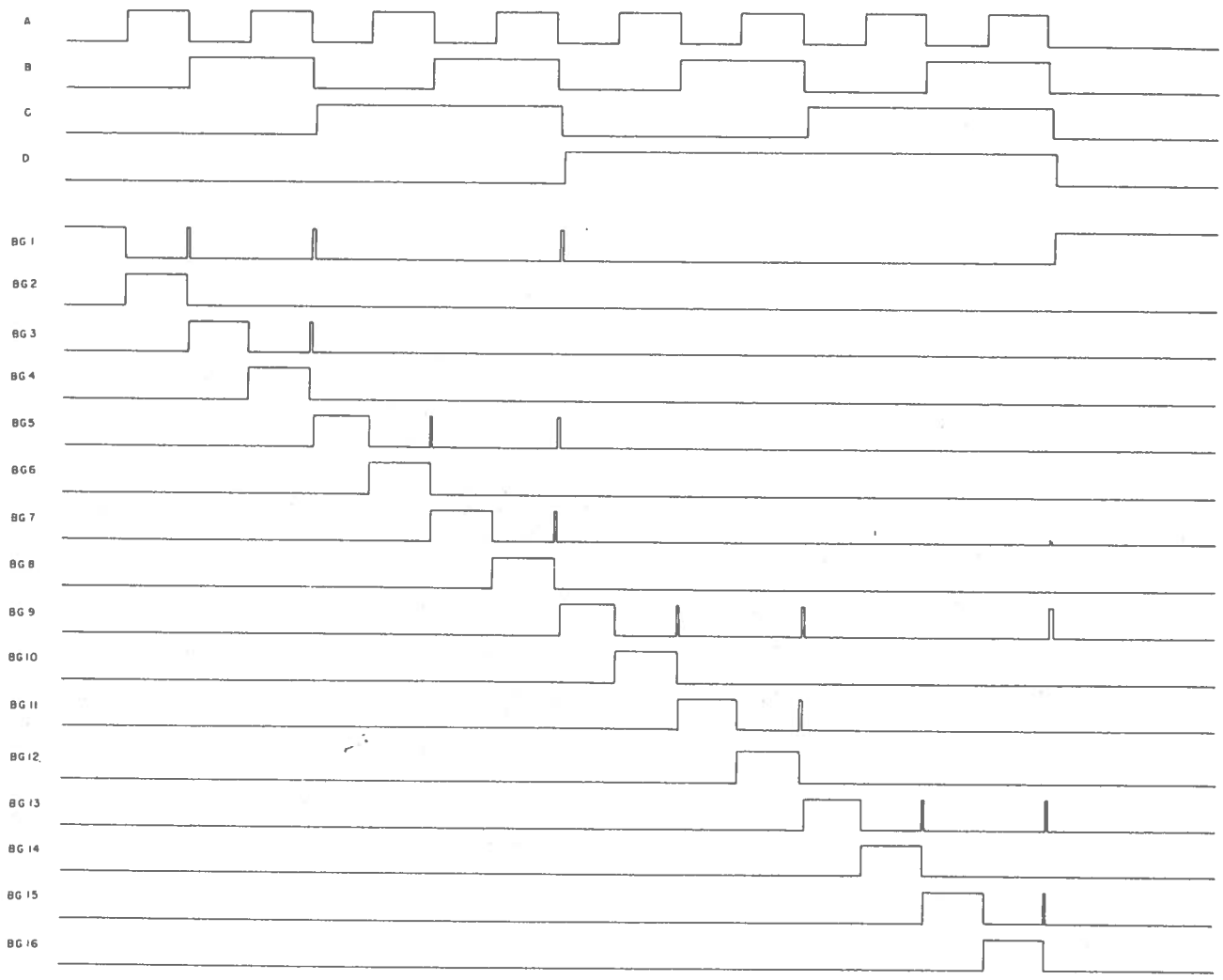
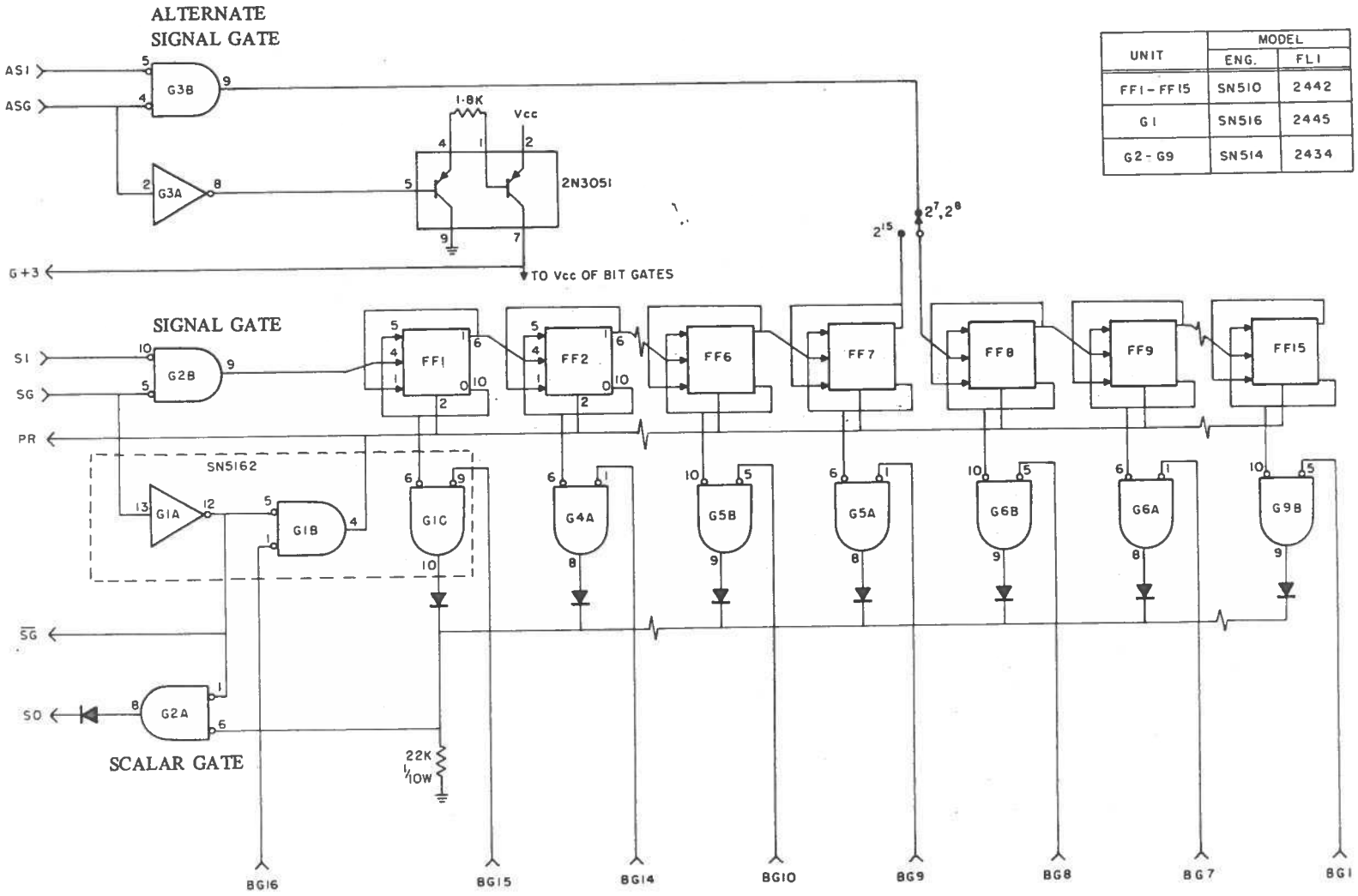


Figure 6 Bit commutator race hazards

Another potentially critical race hazard in the bit commutator occurs when the leading edge of the clock signal lags the leading edge of the read-out-gate signal from the satellite's PCM encoder. Signal *G*, which advances the bit commutator in Fig. 3(*a*), shows the decoding spike at the beginning of the waveform which arises for this condition. The effect of this spike is eliminated by using a monostable multivibrator to keep the bit commutator in a preset condition until well after this spike is gone. To minimize the delay between the output signal from the encoder and the read-out signal from the satellite's PCM encoder, the bit commutator is advanced to the bit-gate 1 position after read-out of any word.

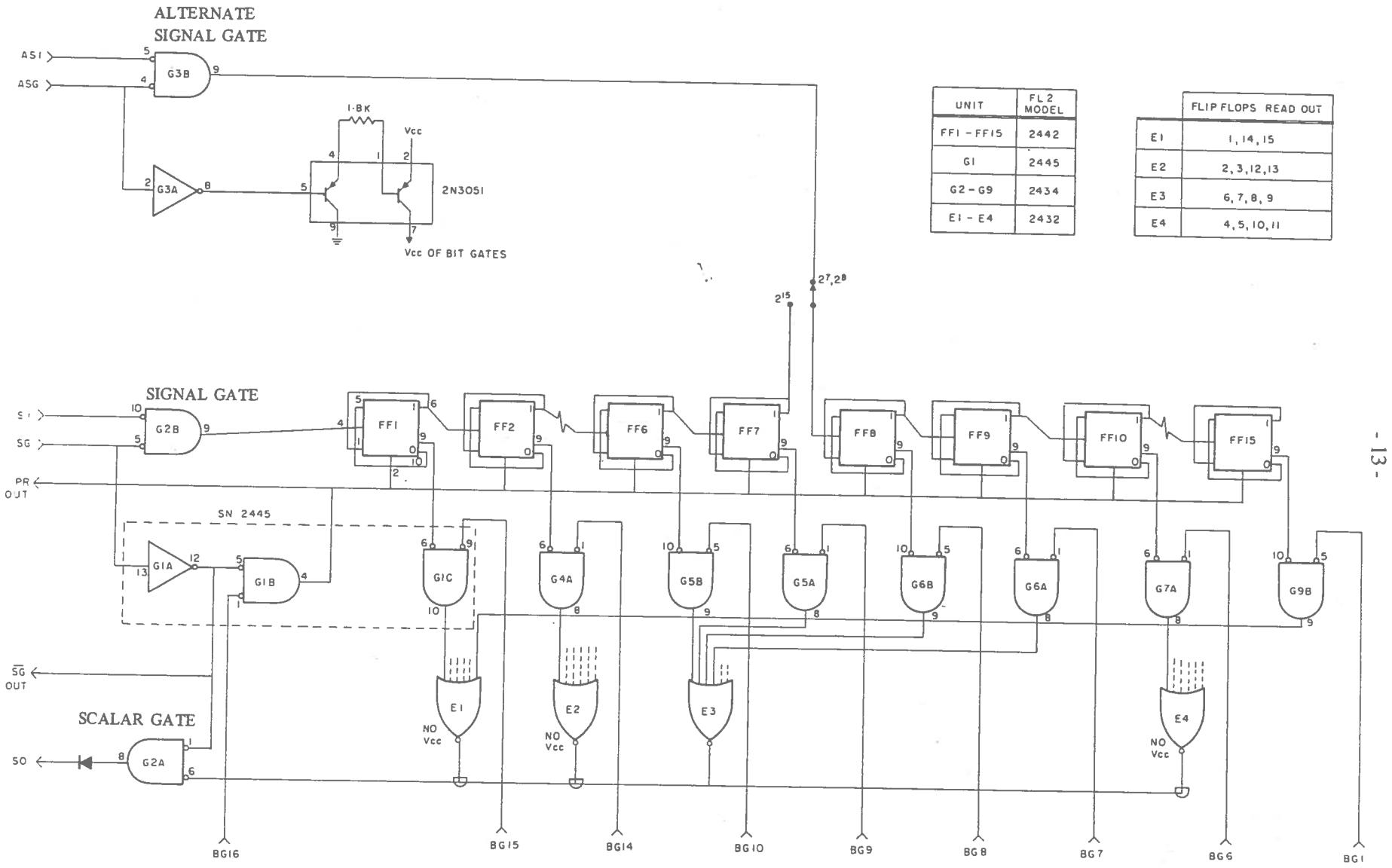
d) Counter

The logic diagram of a typical 15-stage counter for Flight Models 1 and 2 is shown in Fig. 7(*a*) and (*b*), respectively. Pulses from the detector package are fed into the counter



UNIT	MODEL	
	ENG.	FLI
FF1 - FF15	SN510	2442
G1	SN516	2445
G2 - G9	SN514	2434

Figure 7(a) Logic diagram of typical counter (Engineering and Flight Model 1)



UNIT	FL 2 MODEL
FF1 - FF15	2442
G1	2445
G2 - G9	2434
E1 - E4	2432

	FLIP FLOPS READ OUT
E1	1, 14, 15
E2	2, 3, 12, 13
E3	6, 7, 8, 9
E4	4, 5, 10, 11

Figure 7(b) Logic diagram of typical counter (Flight Model 2)

through a 2-input NAND gate, designated *signal gate*, whenever pin 5 on this gate is near ground potential. The gate is closed by placing a nominal 3-V potential on pin No. 5. The timing voltages which control this operation are derived from the word commutator. The output gate, designated *scalar gate* in the figure, is controlled by the complement of the signal-gate signal so that, when the input gate is open, the output gate is closed and vice versa. Note that the basic 15-stage counter can be connected to form two separate counters, one comprising eight stages, the other seven. Each of these smaller counters has its own input gate but they share the same output gate, since they are both read out by the same read signal.

At the end of the count cycle, bit gates shown below the flip-flops are used to sense and read out the state of each flip-flop in sequence, beginning with the most significant bit first. Each of the 16 bit-gate signals, from the bit commutator, is applied to one input of the 2-input NAND bit gates. These signals, which are all normally near +3 V, drop to near ground potential, when read-out of the state of the particular flip-flop to which they are connected is required. The outputs of the 15 bit gates are fed into the output scalar gate through microminiature isolating computer diodes and a 22-kΩ pull-down resistor, which form a 15-input OR gate. Bit-gate signal 16 and the complemented signal-gate signal for that particular counter are applied to a 2-input NAND gate which generates a clearing pulse for the entire counter in preparation for a new counting sequence. Since bit-gate operation is required only during read-out, power to these gates is turned off during the counting cycle. This means that only 15 bit gates are consuming power at any given time since only one word is being read out at any given time. This is accomplished by a dual pnp transistor, 2N3051, which is controlled by the read-out signal gate for that particular counter. This results in an over-all power saving of about 300 mW. This technique is feasible because measurements show that the impedance of the input to these gates is independent of the presence or absence of V_{cc} on these gates; consequently, conventional loading rules apply.

The counter design for the Flight Model 2, Fig. 7(*b*), was modified to replace the 15 diodes with four type SN2432 integrated circuits in a collector-OR configuration to form a 15-input NOR gate. The reason for this modification is discussed in the section on noise immunity.

e) Frame-Sync and Parity Generator

The frame-sync pattern is introduced into the output bit stream by using outputs from the bit commutator to gate *zeros* and *ones* at the appropriate times, Fig. 8(*a*). Since the frame-sync pattern must contain an even parity bit to make it unique, the odd parity generator is inhibited during read-out of the first word as described below.

The parity generator, shown in Fig. 8(*b*), consists of one binary-connected flip-flop and three 2-input NOR gates. The timing waveforms are shown in Fig. 3(*a*). Before

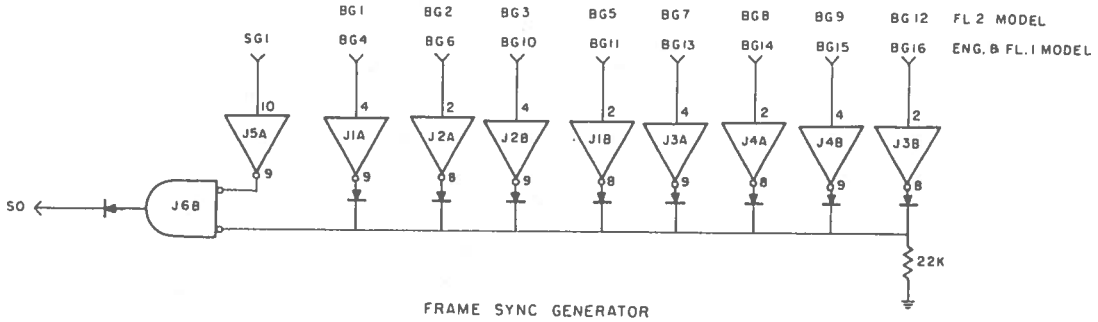


Figure 8(a) Logic diagram of frame sync generator

UNIT	MODEL		
	ENG.	FL 1	FL 2
FF 1	SNR510	2442	2442
J1 – J8	SNR514	2434	2434

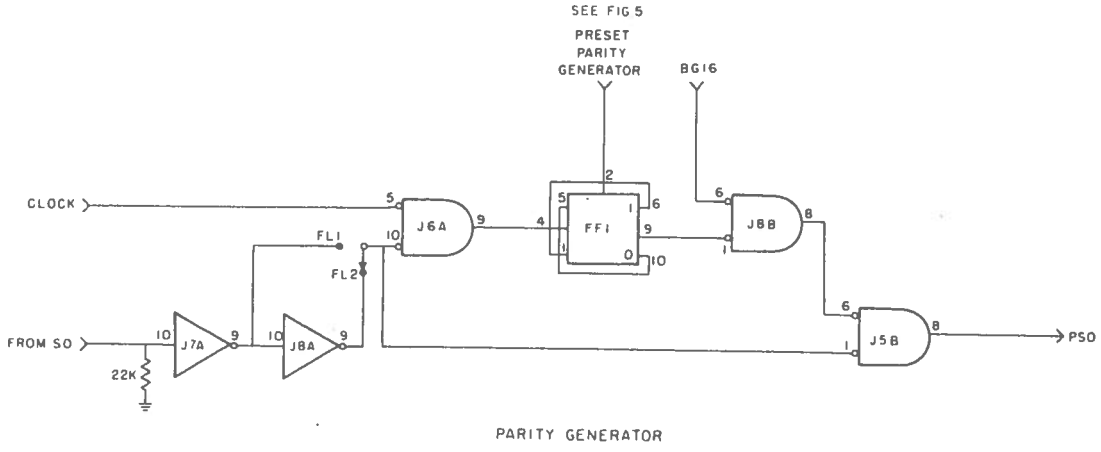


Figure 8(b) Logic diagram of parity generator

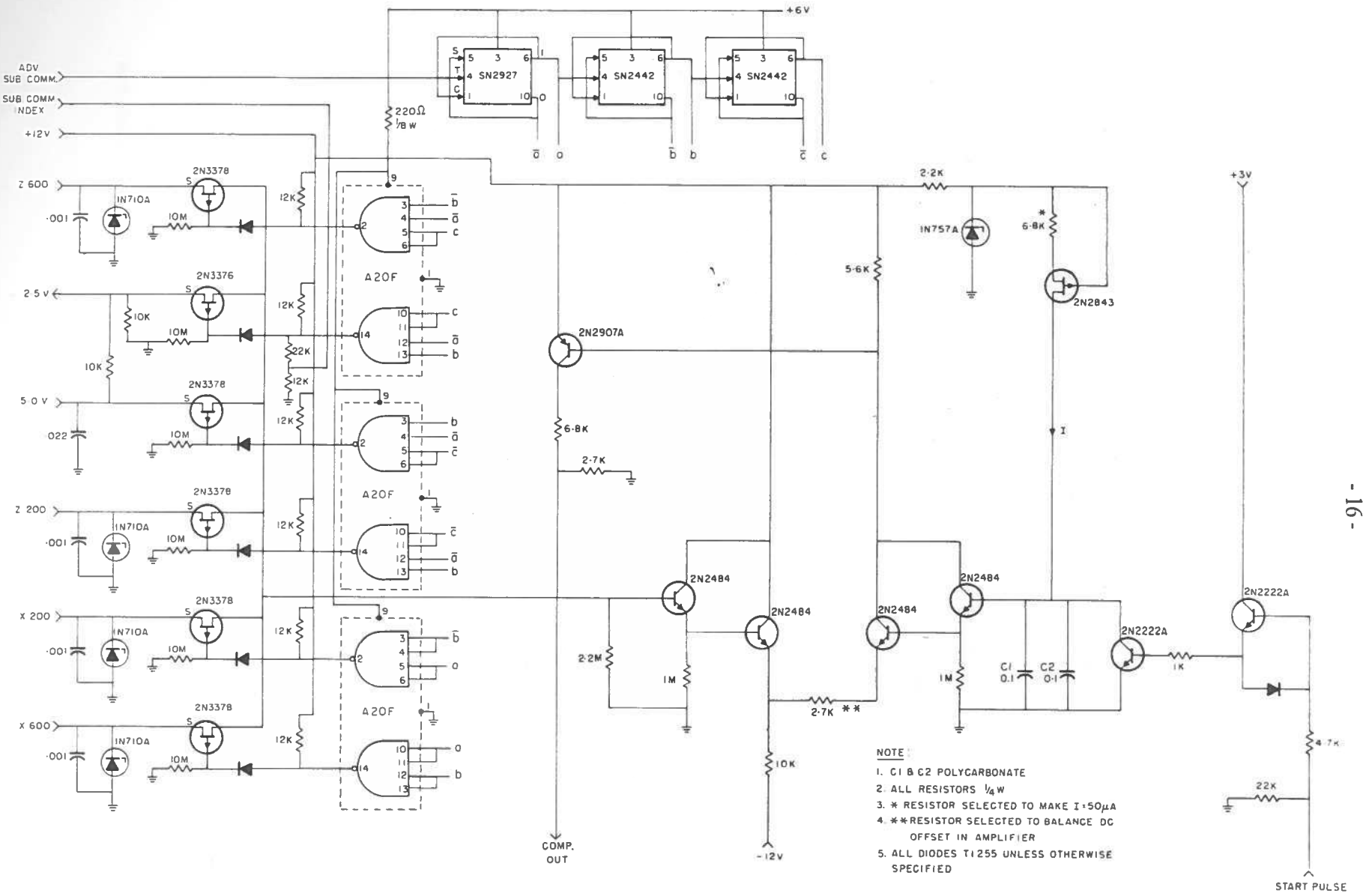


Figure 9 Circuit diagram of analog subcommutator and analog-digital converter

read-out of a word this flip-flop is preset to the zero-state. This flip-flop is driven by the output (0) of a 2-input NOR gate whose inputs are the binary word (N) being read out and the clock (B). In this way the flip-flop is complemented on the arrival of a *zero* and remains unchanged during the receipt of a *one*. Therefore, the state of the flip-flop at the end of the 15th bit of information depends upon the number of *ones* or *zeros* in the first 15 bits. This state (P) is then gated (J) into the output binary data stream as the 16th bit by a 2-input NAND gate. Note that for word 1, the frame-sync pattern, the insertion of a parity bit into the output stream is inhibited by the presence of a fixed *one* (N) during the 16th bit; i.e., the 16th bit of word 1 is a *one* bit regardless of the output of the parity generator. Therefore, a unique frame-sync pattern is possible by choosing one which has an even number of *ones* and *zeros* ending in a *one*. Although race hazards occur at point N these are completely removed at point 0 by the clock signal B as is evident from the timing diagrams in Fig. 3(*a*).

f) Analog Subcommutator

The 6-channel 0–5 V multiplexer, Fig. 9, uses three RCTL flip-flops, three DTL decoder-drivers and six p-channel junction field-effect transistors. Since RCTL is a current-source logic form and DTL is a current-sink logic form, logic level and driving compatibility between these particular logic devices must be determined. In particular, the output transistor in the 2N2442 flip-flop when saturated, must be capable of sinking the current flowing out of the DTL inputs. The maximum current that must be sunk varies from 1.1 mA to 2.6 mA, in the worst case, at maximum voltages of 0.9 to 1.3 V. That the SN2442 is capable of this performance is shown in Fig. 10, where the output voltage across a saturated output transistor in the flip-flop is plotted against an externally introduced current into the collector of the output transistor.

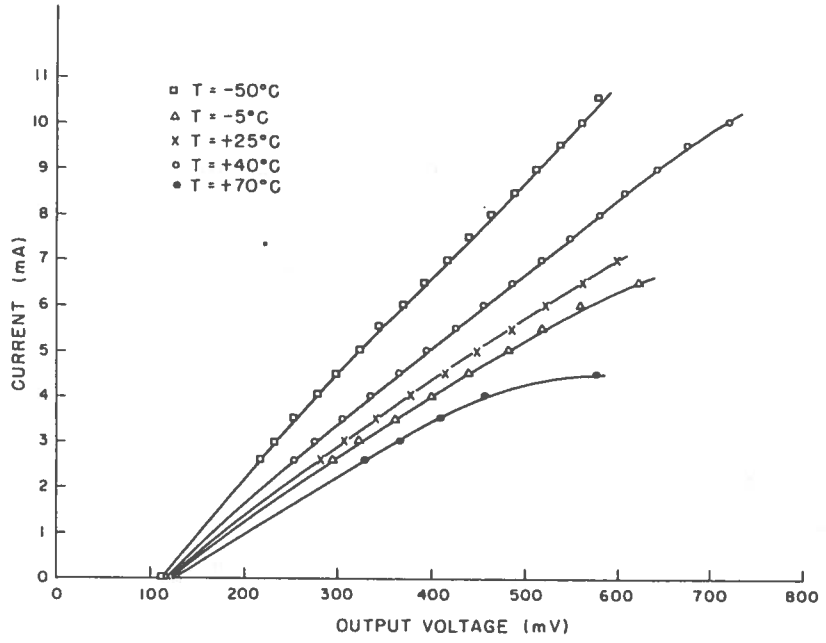
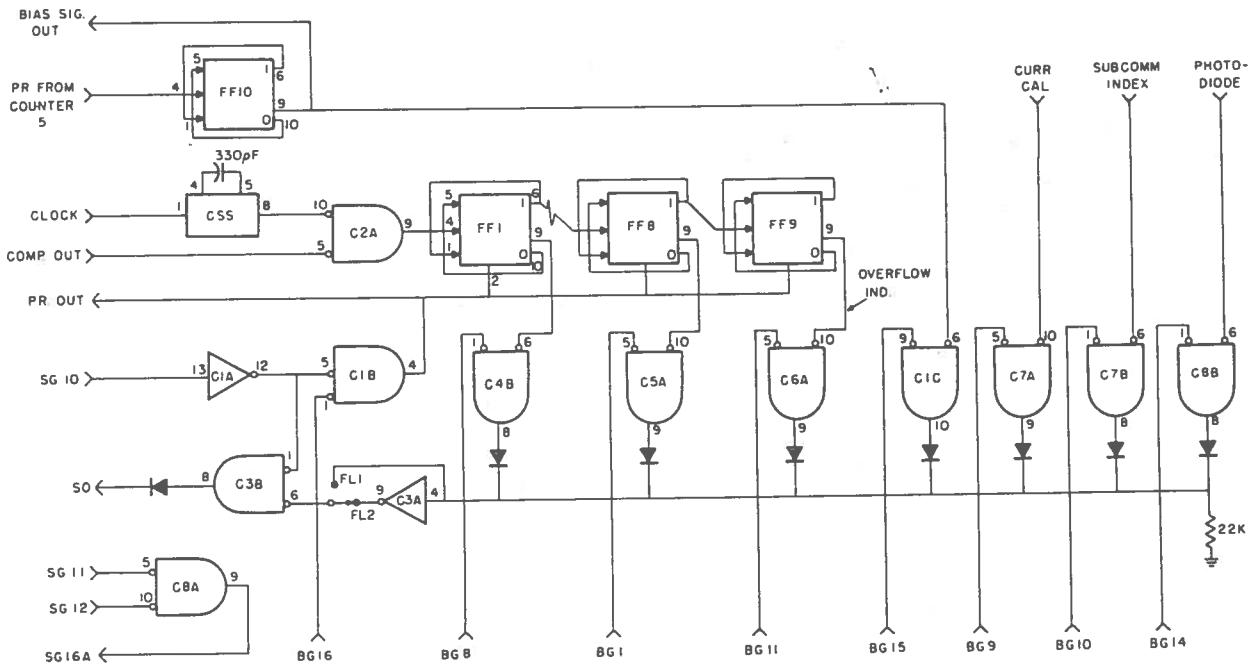


Figure 10 Sinking capability of SN2442



UNIT	MODEL		
	ENG	FL1	FL2
FF1 - FF10	SNR510	2442	2442
C1	SNR516	2445	2445
C2 - C8	SNR514	2434	2434
CSS	SNR518	2438	2438

Figure 11 Logic diagram for flag bit data and ADC counter

g) Analog-Digital Converter

Directional information is provided by digitizing four magnetometer voltages (0–5 V) at a rate of four conversions per second. This low rate, coupled with the fact that the clock supplied by the PCM encoder is stable to within 1 part in 10^6 over the operating temperature range, permitted a relatively low-power ramp-type converter to be used.

Circuit timing is shown in Fig. 3(*b*). The preset pulse from counter 14(Y) begins the conversion cycle by starting the ramp generator (Z) which opens the input gate of the 8-stage binary counter to clock pulses. A differential amplifier compares the selected analog voltage with the linearly rising voltage from the ramp generator and turns off the input gate to the counter when these two voltages become equal. The accumulated count, Fig. 11, is then proportional to the analog voltage and is read out as word 10A.

Circuit details of the analog–digital converter (ADC) are shown in Figs. 9 and 11. The constant-current source is a suitably biassed p-channel junction type silicon field-effect transistor. Circuit parameters of this ramp generator are determined by the clock frequency of 11.52 kHz; for example, an 8-stage counter, accumulating 11,520 pulses per second, will overflow in 22.2 msec. Therefore, the ramp voltage should rise from 0 to 5 V in less than 22 msec if the counter is not to overflow while digitizing a 5-volt magnetometer signal.

Constant-current sources with zero temperature coefficient can be made for particular values of constant current by selecting the type of field-effect transistor used. Space limitations dictate a small capacitor. However, for a fixed charging rate, the smaller the capacitor the smaller the value of the constant-current source. If this becomes too small ($< 10\ \mu A$) stability problems can arise due to leakage – radiation-induced or otherwise. A design compromise was made which resulted in the choice of a 50-μA constant-current FET source (2N2842) charging two 0.1-μF polycarbonate capacitors, C_1 and C_2.

The comparator consists of a conventional discrete-component differential amplifier with Darlington inputs. Although monolithic differential amplifiers were available at the time, they consumed too much power for this application. Recently low-power monolithic operational amplifiers have become available, e.g., National semiconductor type NH0001 which consumes 2 mW. These should certainly be considered in any future modification.

Typical input-output characteristics at three temperatures for voltages near 0 and 5 V are shown in Figs. 12(*a*) and (*b*) for Flight Model 2. The quantization error in the converter is about ±0.2%. Measurements have shown that short-term stability is good. A consistent difference of 12 mV (0.2%) was noted between tests conducted at the Radio and Electrical Engineering Division of the National Research Council (NRC) in Canada and tests conducted at the Goddard Space Flight Centre (GSFC) in Greenbelt, Maryland, about one month later. This difference may be due to the different digital voltmeters used or differences in the encoder grounding system. Even were this difference solely due to

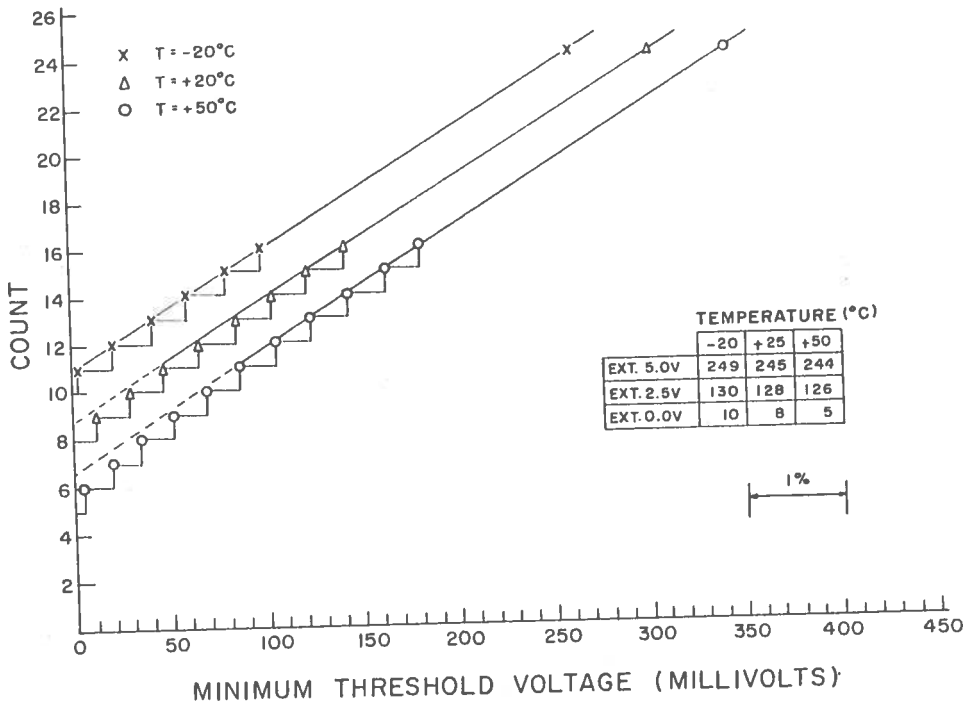


Figure 12(a) Input-output characteristic near 0 volts input

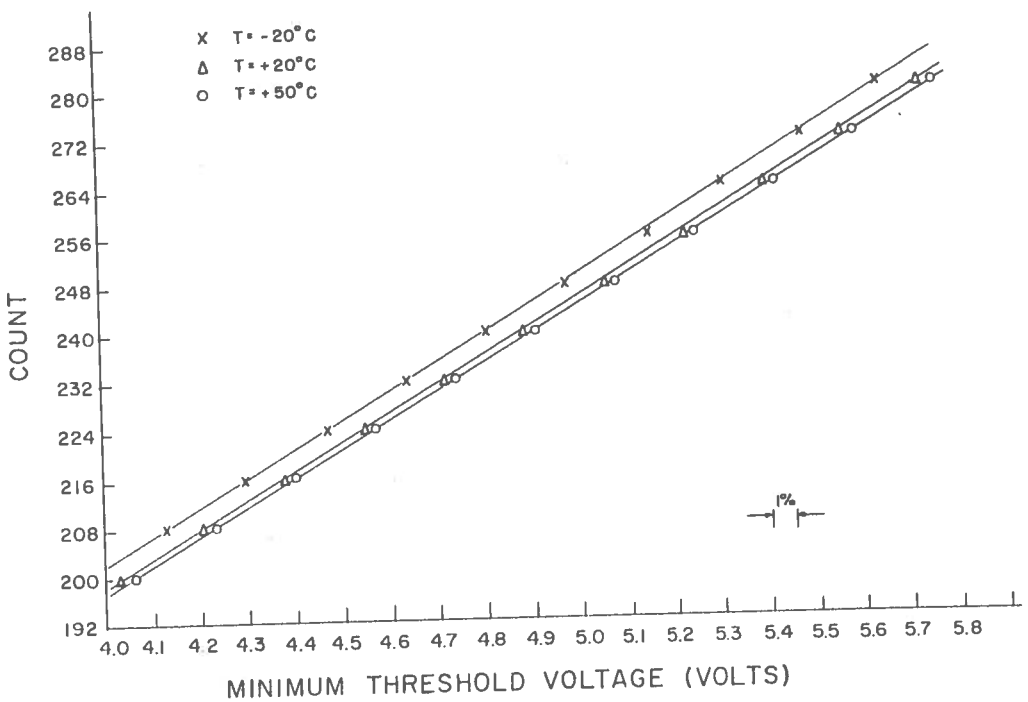


Figure 12(b) Input-output characteristic near 5 volts input

experimental errors, it would not be wise to depend only upon ground calibration for a long period of time, such as one year. Consequently, in-flight calibration is used. Once every eight frames a +5-volt and +2.5-volt reference signal is sampled and digitized. This calibration is used to compute the input-output characteristic which is assumed to be linear. Under this condition the maximum expected error is shown by the solid line in Fig. 13. Note that errors due to nonlinearities exist near 5.0 volts at +40°C and near 0 volts at +20°C. A converter accuracy of ± 1% was the design goal. Measurements show that this was attained everywhere except below about 250 mV at 20°C. This is not serious since it occurs near the extremity of the scale; i.e., full-scale magnetometer readings occur near 0 and 5.0 V with zero gauss occurring at +2.5 V.

Differences between the four magnetometer channels amount to only a few millivolts and contribute a negligible error.

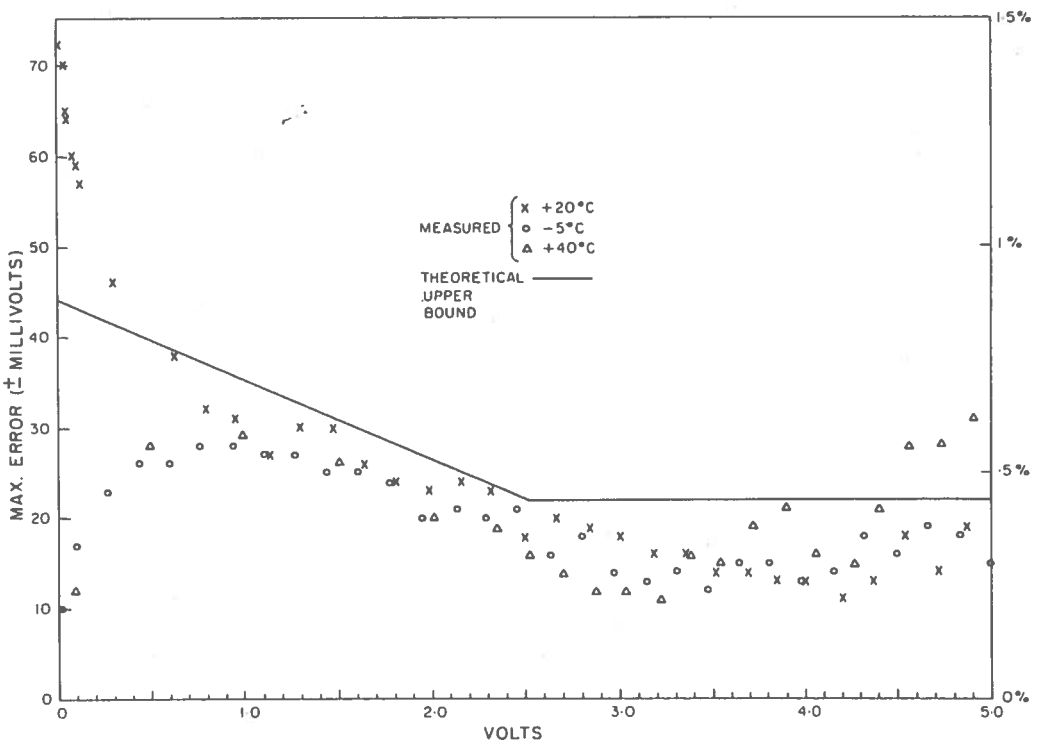


Figure 13 Maximum error expected with in-flight calibration of ADC

h) Noise Immunity Considerations

Noise immunity is one of the important elements of reliable digital design. The dc noise margin of the integrated circuit family used is 200 mV for fully loaded gates. Driving capability can be sacrificed for increased dc noise margin. Therefore, wherever practical, three or fewer gates were driven from any collector node. A collector node in this series of integrated circuits is capable of driving 5 gates.

Noise margin in RCTL circuits is greater for negative-going signals than for positive-going signals. Consequently, signal pulses on lines which are susceptible to impulsive interference pickup are transmitted as short negative-going pulses from 3 V to ground. This was particularly important where dc pulses from the detector package had to be transmitted over an open cable about 2 feet long to the encoder package. This cable is harnessed with another bundle of wires, some of which carry interference-producing signals.

The Engineering and Flight Model 1 of the data encoder use 15 microminiature isolating computer diodes between the 15 bit read-out gates and the output signal gate of each counter. Measurements show that the voltage drop across one of these diodes is equivalent to the loading which would be produced by three gate inputs. This loading with the 22-kΩ pull down resistor and the input load of the output signal gate combines to fully load the bit gates. In addition, output voltage available to the output signal gate is reduced further by the voltage drop across the 2N3051 switching transistor which controls the application of V_{cc} to the bit gates. For the existing 25-mA load, this voltage loss varied from 72 to 179 mV depending upon the particular transistor (2N3051) used. Therefore, the noise margin at this point was reduced from about 200 mV to between 127 and 21 mV. This loss in noise margin is partially offset by selecting output signal gates with lower than average input requirements. Although tedious, this selection is relatively simple since all the RCTL integrated circuits purchased for use in flight models are individually characterized; i.e., a computer print-out is supplied with each integrated circuit listing all pertinent parameters. A typical listing is shown in Fig. 14.

Although no trouble has been experienced in either the Engineering or Flight Model 1 because of this reduced noise margin at the input to the output signal gates, a modification was made in Flight Model 2 in which the 15 diodes were replaced by four type SN2432 integrated circuits. These are 4-input NOR gates. This eliminates the voltage loss across the diodes, leaving only the loss in V_{cc} across the switching transistor. This loss in V_{cc} is more than overcome by the fact that the bit gates, which are capable of driving five loads, drive only one load. Diode OR gates continue to be used to combine the outputs from the scalar gates of the counters. These output counter gates are not switched off so that loss in V_{cc} does not reduce the noise margin at this point. However, as an additional safety factor, output gates were selected which had loaded output voltages one standard deviation above the average voltage.

LISTING OF UNITS

DEVICE SN2434 DATE CODE LOT NO. 1614 4117 DATE READ06/08/66 TIME 300 HOUR JOB NASA

ALL UNIT READINGS ARE INCLUDED IN THE LISTING. AN L TO THE RIGHT OF A PARAMETER READING IS A FAILURE AND CAN BE ACCEPTED AS AN ACCURATE READING. AN X TO THE RIGHT OF A PARAMETER IS A FAILURE BUT MAY NOT BE AN ACCURATE READING.

	TEST	PARAGRAPH	MIN	MAX		MIN	MAX
PAR 1	INPUT CURRENT PIN 1	VCC OF 6V			UA		
PAR 2	INPUT CURRENT PIN 2	VCC OF 6V			UA		
PAR 3	OFF VOLTAGE PIN 8	VCC OF 6V			V		
PAR 4	OFF VOLTAGE PIN 9	VCC OF 6V			V		
PAR 5	OFF VOLTAGE PIN 8	VCC OF 6V			V		
PAR 6	OFF VOLTAGE PIN 9	VCC OF 6V			V		
PAR 7	ON VOLTAGE PIN 8	VCC OF 6V INPUT PIN 1			V		
PAR 8	ON VOLTAGE PIN 8	VCC OF 6V INPUT PIN 2			V		
PAR 9	ON VOLTAGE PIN 8	VCC OF 6V INPUT PIN 6			V		
PAR 10	ON VOLTAGE PIN 9	VCC OF 6V INPUT PIN 4			V		
PAR 11	ON VOLTAGE PIN 9	VCC OF 6V INPUT PIN 5			V		
PAR 12	ON VOLTAGE PIN 9	VCC OF 6V INPUT PIN 10			V		
PAR 13	INPUT CURRENT PIN 4	VCC OF 6V			UA		
PAR 14	INPUT CURRENT PIN 5	VCC OF 6V			UA		
PAR 15	INPUT CURRENT PIN 6	VCC OF 6V			UA		
PAR 16	INPUT CURRENT PIN 10	VCC OF 6V			UA		

UNIT NUMBER	PAR 1	PAR 2	PAR 3	PAR 4	PAR 5	PAR 6	PAR 7	PAR 8	PAR 9	PAR 10	PAR 11	PAT 12	PAR 13	PAR 14	PAR 15	PAR 16	PAR 17	PAR 18
222	84.10	85.90	5.960	5.960	3.980	3.970	.0780	.0790	.0960	.0830	.0830	.1000	82.00	80.90	82.20	83.80		
223	69.10	68.40	5.960	5.960	3.710	3.760	.0740	.0750	.0750	.0760	.0750	.0750	70.80	71.60	69.30	75.40		
224	74.30	74.90	5.960	5.960	3.810	3.810	.0590	.0600	.0760	.0650	.0820	.0630	72.80	72.80	74.00	77.80		
225	71.00	70.40	5.960	5.960	3.720	3.720	.0670	.0690	.0890	.0920	.0920	.0720	68.30	73.00	69.20	72.20		
226	68.70	67.20	5.960	5.960	3.720	3.750	.0760	.0770	.0770	.0810	.0810	.0820	69.80	70.30	69.00	74.00		
227	77.10	76.40	5.960	5.960	3.890	3.910	.0840	.0860	.0890	.0890	.0970	.0870	77.60	78.40	78.10	82.70		
228	68.00	68.20	5.960	5.960	3.680	3.700	.0610	.0600	.0580	.0730	.0530	.0690	70.30	69.70	67.50	72.10		
229	71.90	71.70	5.960	5.960	3.780	3.800	.0680	.0690	.0690	.0690	.0690	.0690	73.30	73.70	71.90	77.50		
230	76.50	76.00	5.960	5.960	3.870	3.880	.0720	.0900	.0730	.0770	.0750	.0750	77.40	78.40	76.50	82.70		
231	73.70	73.20	5.960	5.960	3.900	3.840	.0780	.0640	.0820	.0800	.0750	.0630	74.20	74.80	72.40	77.50		
232	86.80	89.70	5.960	5.960	4.000	4.080	.0710	.0810	.0630	.0770	.0950	.0950	83.80	83.40	83.60	87.50		
233	75.80	74.70	5.960	5.900	3.870	3.870	.0600	.0790	.0690	.0700	.0730	.0650	76.50	76.80	76.10	81.10		
234	60.80	60.10	5.960	5.960	3.470	3.470	.0530	.0550	.0540	.0590	.0580	.0580	60.30	61.70	60.30	65.20		
235	73.20	72.70	5.960	5.960	3.750	3.760	.0690	.0700	.0680	.0740	.0720	.0710	70.30	71.50	73.00	75.80		
236	86.40	86.00	5.960	5.960	3.900	3.900	.0890	.0720	.0740	.0730	.0930	.0740	80.90	80.10	83.90	83.80		
237	67.80	67.40	5.960	5.960	3.690	3.710	.0810	.0750	.0820	.0680	.0670	.0680	69.50	69.80	67.90	73.30		
238	70.00	71.00	5.960	5.960	3.690	3.700	.0600	.0610	.0760	.0770	.0590	.0610	68.20	68.40	69.30	71.70		
TOTALS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

TOTAL UNITS FAILING AT LEAST ONE PARAMETER 0

TOTAL UNITS IN DATA SET 234

	AVERAGE	STANDARD DEVIATION
PARAMETER NUMBER 1	71.0085	5.7900
PARAMETER NUMBER 2	71.0009	6.2021
PARAMETER NUMBER 3	5.9581	.0182
PARAMETER NUMBER 4	5.9585	.0072
PARAMETER NUMBER 5	3.7440	.1255
PARAMETER NUMBER 6	3.7565	.1282
PARAMETER NUMBER 7	.0763	.0160
PARAMETER NUMBER 8	.0780	.0161
PARAMETER NUMBER 9	.0770	.0165
PARAMETER NUMBER 10	.0812	.0151
PARAMETER NUMBER 11	.0804	.0154
PARAMETER NUMBER 12	.0792	.0154
PARAMETER NUMBER 13	70.8825	5.6035
PARAMETER NUMBER 14	71.3303	5.5006
PARAMETER NUMBER 15	70.8838	5.7710
PARAMETER NUMBER 16	74.8423	5.7087

Figure 14 Typical computer parameter listing for integrated circuits

Mechanical and Thermal Design

Good mechanical design for spacecraft packages demands

a) Small size and weight
b) Easy replacement or maintenance at the integrated circuit level
c) Protection against vibration
d) Good heat removal

Flight Model 1 of the encoder contains 433 silicon integrated circuits, 248 miniature diodes, 67 resistors, 16 transistors, 14 dual transistors, 14 capacitors, and 5 zener diodes. Flight Model 2 of the encoder is identical, with the exception that an additional 56 integrated circuits were used to replace 204 of the diodes. After considerable testing, some of which will be described later, it was decided that the above requirements could best be achieved by using $\frac{1}{16}$-inch double-sided printed-circuit boards on which the integrated circuits are inserted into rectangular holes which have been made in the boards. Space is conserved by placing two integrated circuits into each hole, the leads being soldered to lands on the printed circuit board. Interface connections, (i.e., connections from one side of the board to the other) are made by passing wires through holes of 13 thousandths diameter swaging on either side and soldering in place.

Input and output connections to the board are made by wires which are soldered and firmly attached to the lands located along two edges of the board. The completed board is then cleaned, tested, and inserted into the mould shown in Plate V where it is encapsulated with a silicone encapsulating resin. This encapsulant cushions the integrated circuits and provides a thermal condition path for heat removal. The final board then takes on the appearance of a wafer, 5.8 inches long by 2.4 inches wide by $\frac{1}{8}$ inch thick, with up to 24 leads coming off one edge and from 5 to 8 leads coming off the narrow edge. Six stages in the fabrication of a counter board from Flight Model 2 are shown in Plate II. Note that only the top side of the board is shown. A total of nineteen $\frac{1}{16}$-inch epoxy boards, 18 of which are double-clad printed circuit boards, are used to mount and interconnect all the integrated and discrete circuits in the encoder. Repairs and modifications are facilitated and connections are minimized by partitioning the system into several logical functions, each of which is contained on one of six board types. These are counter boards (of which there are fourteen), one word-commutator board, one bit-commutator board, one housekeeping board, one sync board, and one discrete component board. These boards all have the same dimensions, 5.6 inches X 2.2 inches X 0.625 inch. The appearance of these board types for the three encoder models is shown in Plates III and IV.

Encapsulating the board in Silastic serves two purposes – it provides good heat conduction and protection from vibration and shock. Sinusoidal vibration experiments conducted with an electrically driven vibration table, a stroboscope, and a stereo microscope verified the mechanical integrity of this method of attaching the integrated circuits to the printed circuit boards. The vibration levels used were greater than those specified for spacecraft packages. A printed circuit board with integrated circuits, resistors, and diodes was sinusoidally vibrated in each of three axes and the stereo microscope was used to examine the individual components on the board. A section of the board with components had been potted. The audio oscillator driving the vibration table was also used to synchronize the strobatac which illuminated the test board. No resonances were observed in any of the components, potted or otherwise.

In addition, pull tests perpendicular and parallel to the board were conducted on the individual integrated circuits. In no test did a pull of less than 2 lb cause failure. In some tests, failure did not occur until a pull of 8 lb was reached. For these tests failure was mechanical in nature – either the leads broke at the package or separated from the solder joints at the lands. As a result of these and other tests a great deal of confidence was gained in this method of mounting individual integrated circuits.

Since a spacecraft operates in a vacuum, thermal dissipation can be a problem. The extent of this problem in the data encoder was investigated by mounting $\frac{1}{10}$-W resistors, to simulate the power dissipated by an integrated circuit, on a dummy board. A bead thermistor was mounted beside the resistor to monitor its temperature. The unit was then encapsulated in Silastic and operated in a vacuum, where temperature readings were taken for various levels of power dissipation. For anticipated power levels of 2 mW/gate a temperature differential of less than 1°C was recorded. For a power dissipation of 34 mW or 17 times the anticipated level a temperature differential of 13°C was recorded. This would still be within the encoder temperature limits. It was concluded that the thermal design was adequate.

After encapsulation, the 19 wafers are stacked one on top of the other and held together by five rods which pass through holes located along three edges of the boards. These wafers are interconnected by the two interconnection printed circuit boards shown in Plate VI. On these boards two holes are provided for each lead; one allows the lead from the wafer to be brought through to the front and soldered into an eyelet located in an adjacent second hole. These eyelets are interconnected by a printed circuit pattern. There are still a considerable number of wires, which carry signals from one interconnection board to the other. Original assembly of the stack is done on a wafer-by-wafer basis

beginning at the bottom; i.e., the bottom wafer is soldered in before the next wafer is placed on top. The 19 wafers with their interconnection boards are mounted inside an aluminum shielded box with over-all dimensions of $7\frac{1}{2}$ inches X 4 inches X $3\frac{1}{2}$ inches. The over-all weight of the encoder is 4 lb, of which 2 lb is due to the box.

It is felt that the interconnection method described above offers compactness and reliability with relatively easy maintenance. Repair is conducted on an individual integrated circuit basis. Removal of any wafer in the stack can easily be done in 20 minutes. The operation is simple and straightforward, requiring at most the unsoldering of 32 wires, and the removal of the 5 rods. The wafer is then pulled out. After the necessary repairs or modifications are made on the board, it can be re-inserted in about 30 minutes in a simple and straightforward fashion, even though it is necessary to pass about 24 semi-flexible leads, each about 1 inch in length, through 24 holes located in an interconnection board about 2.5 inches away at the end of a slot, which is about $\frac{1}{4}$ inch in width. To simplify this re-insertion problem, the comb shown in Plate V is used. The teeth in the comb are passed through their respective holes in the interconnection board until the tips emerge at the side of the encoder opposite the large interconnection board. The tips of the teeth have small holes drilled into them; it is into these holes that the wires from the repaired board are inserted and soldered. The comb is then pulled back out again bringing the wires and wafer with it. Wafers have been removed and re-inserted in this fashion on several different occasions with no difficulties.

Reliability

Reliability is the most important single factor in the design of equipment for satellite use. The SN51 series of integrated circuits is available in the three different grades of reliability listed below.

SN Series	SNR Series	NAS-51 Series
SN 510	SNR510	
SN 511	SNR511	SN2927
SN 5112	SNR5112	SN2442
SN 512	SNR512	SN2432
SN 513	SNR513	SN2433
SN 514	SNR514	SN2434
SN 516	SNR516	
SN 5162	SNR5162	SN2445
SN 518	SNR518	SN2438

The engineering model was constructed with integrated circuits of both the SN and the SNR series. Both flight models were constructed with the 51 series of integrated circuits meeting NASA specifications; in particular, the NAS-51 specification [4]. Trouble with the NAS-51 series has been minimal and will be discussed in greater detail in a later section.

With the NAS-51 series the manufacturer provides recorded parameter data for individual integrated circuits in a format shown in Fig. 14. When the circuits are received from the manufacturer, they are subjected to visual and electrical inspection tests. Each circuit is examined first under a stereo microscope for mechanical defects and subjected to simple GO – NO GO functional electrical tests at room temperature. The purpose of these tests is to uncover damage that may have occurred during shipping or handling after the final electrical tests have been conducted by the manufacturer. Acceptable circuits are allocated and installed on the printed circuit boards. Traceability of each circuit is maintained with written and photographic records; i.e., the history of every integrated circuit used on the flight models is recorded.

For critical functions, integrated circuits have been hand-picked using the recorded data parameters provided by the manufacturer; e.g., where loading is critical, units with lower than average input current requirements have been selected, provided that the units do not exhibit anomalies in other data parameters.

For any particular lot, the manufacturer's automated test procedure provides the average and the standard deviation for all data parameters. Although it is tempting to select units with the lowest input current requirements for critical loading areas, this is never done. Although the author knows of no work showing a correlation between the MTBF of a unit and its deviation from the average, it is felt intuitively that units exhibiting data parameters much better or worse than the average are less reliable. Consequently, circuits for critical areas were selected so that their data parameters did not exceed plus or minus one standard deviation from the average. Therefore, in the example noted above, gates were selected with input current requirements which were not less than one standard deviation below the average. The format in which the data parameters were presented by the manufacturer did not permit rapid selection of units with particular data parameters. It is recommended that future lots be ordered with the data parameters recorded on punched cards. This would make individual circuit selection possible with computer-controlled card sorters.

It is important to re-emphasize the fact that successful operation of the encoder does not depend upon selecting individual integrated circuits. This selection, is, rather, an attempt to use the data supplied by the manufacturer to improve the performance margin of the encoder. Indeed, the engineering model continues to operate satisfactorily, although no attempt was made to select particular units for electrically critical functions.

Radiation Considerations

In choosing components for orbiting spacecraft equipment, the effects of potentially damaging corpuscular radiation must be considered. The radiation resistance of the 51 series of integrated circuit logic elements was determined from,

a) electron and proton radiation measurements reported by the manufacturer, Texas Instruments Ltd. [5],

b) Co^{60} radiation measurements conducted by the Applied Physics Laboratory of the Johns Hopkins University,

and *c)* Co^{60} radiation measurements conducted at NRC.

The average total radiation flux anticipated inside the ISIS-A spacecraft and shell is tabulated below.

Electrons	< 2.2 MeV	Shielded out
	> 2.2 MeV	1.2×10^{10} electrons cm^{-2} day^{-1}
Protons	< 30 MeV	Shielded out
	> 30 MeV	3.6×10^{8} protons cm^{-2} day^{-1}

Accumulated radiation dose over the expected one-year lifetime of the satellite is 4.38×10^{12} electrons cm^{-2} and 1.33×10^{11} protons cm^{-2}. The results from all three sources listed above showed little or no degradation in the electrical characteristics of the 51 series of integrated circuits for an electron flux up to 10^{13} electrons cm^{-2} and a proton flux up to almost 10^{12} protons cm^{-2}. Integrated-flux to failure is from 1 to 2 orders of magnitude greater than the above figures. Therefore, little or no radiation damage is expected for a one-year mission. This is a very conservative estimate since it does not include the additional shielding provided by the $\frac{1}{16}$-inch thick aluminum box or the Silastic encapsulant. In addition, critical subsystems such as the bit commutator, word commutator, sync circuitry, and circuitry for storing housekeeping information have been placed in the center of the stack of 19 wafers. These circuits are then afforded maximum protection from the damaging effects of corpuscular radiation. Consequently, the solid-state particle detectors located in the detector package at the skin of the satellite will determine the radiation-induced lifetime of the experiment, since they are, of course, unprotected from the radiation they must detect. These detectors have varying degrees of resistance to radiation; consequently, some are expected to last longer than others. The particular location of a counter board in the stack is determined by the radiation resistance of the detector supplying pulses to that counter. The more radiation-resistant the detector, the closer to the stack center is its particular counter board located. The discrete-component board is located at the top of the stack since the components on this board are more resistant to radiation than are the integrated circuits.

History of Encoder Performance

Once constructed, satellite equipment must undergo extensive testing. Throughout the testing period, proper equipment operation was verified with a check-out system described elsewhere [6].

A history of the performance of the three encoders is best discussed in terms of the chronological development of the program as shown in Fig. 15.

Engineering Model

This model, which was completed in July 1965, contains 156 integrated circuits from the SN series, 274 from the SNR series, and 3 DTL circuits from another manufacturer. In the first 220 hours of environmental testing between -50°C and +70°C, six units failed — five of the SN series and one of the SNR series [7]. The encoder was integrated into the prototype model of the spacecraft in February 1966. In March 1967 one additional SN circuit failed. No additional failures have occurred.

Flight Model 1

This model, which was completed in September 1967, contains 400 NAS-51 circuits, 33 SNR circuits, and the 3 DTL circuits mentioned above. After 230 hours of operation at temperatures between -50°C and +70°C at NRC, this model was taken to GSFC for qualification testing. Just before these tests, a malfunction developed which affected 8 of the 256 bits that are generated in every frame. This fault, which was intermittent, appearing only at temperatures at or slightly above room temperature, was discovered just before the model's qualification tests at Goddard.

The nature of the problem indicated a long and costly delay since the necessary jigs were not available to effect a repair. Therefore, permission was obtained from the project director to proceed with the random vibration and thermal-vacuum tests with the proviso that the tests might have to be repeated some time in the future. During the week of thermal-vacuum testing the fault appeared for two short intervals of a few minutes each. This suggested either an intermittent fault in a particular integrated circuit or a poor connection leading to that circuit. Upon its return to the Radio and Electrical Engineering building at NRC the suspected integrated circuit was replaced and forwarded to the Failure Analysis Group at the Goddard Space Flight Centre. The analysis disclosed that gold particles on the silicon die surface caused the intermittent condition by short circuiting adjacent metallization paths on the integrated circuit [8]. Recorded observations tended to confirm this diagnosis. Five additional circuits from the same lot were forwarded to the GSFC for nondestructive tests. Flight Model 1 was successfully integrated into the flight model spacecraft at RCA Victor in Montreal on October 3–4, 1967.

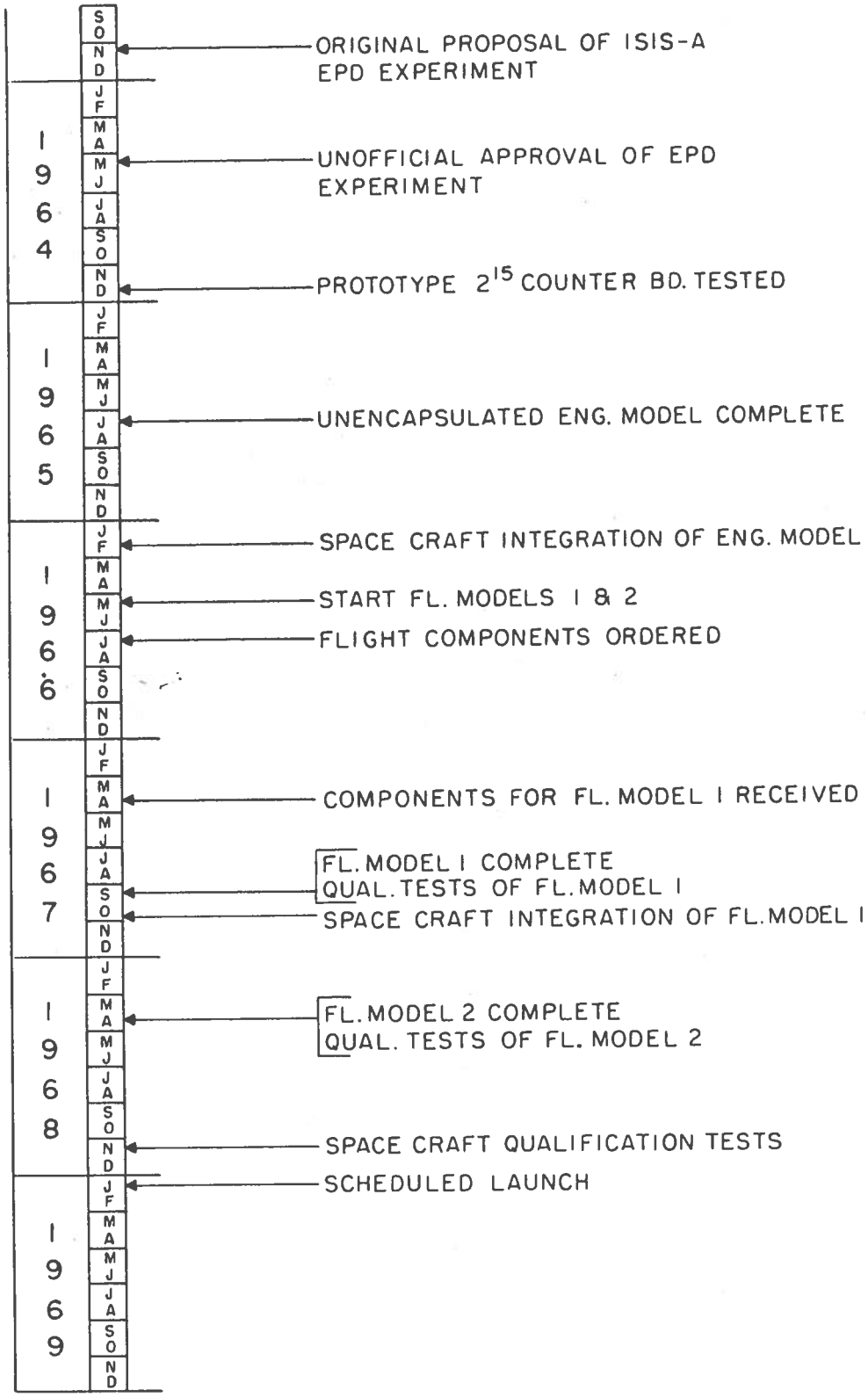


Figure 15 Chronological development of EPD data encoder

Flight Model 2

Construction of Flight Model 2 was begun in October 1967 and completed by April 1968, at which time it was operated successfully for a total of $193\frac{1}{2}$ hours at temperatures between $-20°C$ and $+50°C$. As mentioned previously, this model differs from the first two models in that most of the TI-255 isolating diodes have been replaced by integrated circuit gates. This results in a total integrated circuit count of 492, of which 488 are NAS-51 units. Random vibration and thermal-vacuum qualification tests were completed successfully on this model at GSFC from April 22–27, 1968, and a report describing its performance during these tests has been completed [9]. Flight Model 1 was replaced by Flight Model 2 on the flight spacecraft prior to spacecraft qualification tests at GSFC in September 1968. Flight Model 2 of the encoder operated successfully throughout the qualification tests conducted on the ISIS-A spacecraft.

General Comments

It is clear that meticulous attention to detail is necessary for the successful development of satellite equipment. Although many details were necessarily omitted from this report, an attempt has been made to give the prospective designer of spacecraft equipment a feel for the main factors that must be considered if success is to be attained. In the concluding paragraphs some observations of a more general nature will be made.

A prospective experimenter should be aware of the exhaustive testing that spacecraft packages must undergo before launching. Packages undergo many hundreds of hours of testing before they are integrated into the spacecraft. After integration, packages undergo many additional hundreds of hours of testing on the spacecraft. The flight model of the EPD experiment will have undergone 15 months of testing on the satellite before launch.

Long delivery times for components of high-reliability are the rule rather than the exception. For example, a one-year delay occurred between the time that flight-quality integrated circuits were ordered and enough were received to complete one flight model. Work had to be carefully scheduled to minimize the effect of this long delay on the overall progress of the EPD data encoder.

One of the more important elements that must be considered in any satellite experiment is the long time between its conception and its execution. For example, five years will have elapsed between the original proposal of the ISIS-A EPD experiment and the currently scheduled launch date (January, 1969). Over such a long time span new requirements or constraints, which are beyond the designer's control, can arise. The system design, therefore, must be kept as flexible as possible for as long as possible if lengthy and costly delays are to be avoided.

One of these unforseeable constraints arises from technological improvement. For example, after the engineering model of the encoder was completed the integrated circuit

manufacturer introduced a new improved flat package for his high-reliability NAS-51 line. This new package was slightly larger than the old package in several dimensions; this prohibited the use of crimped leads for stress relief as had been done in the engineering model. Although this change has not led to any measurable detrimental effects, this might not always be the case.

In another instance the manufacturer drastically increased the body dimensions of his line of microminiature computer diodes (over 500 are used in the engineering and flight 1 models), in order to increase their thermal time constant. The need for a large number of these diodes in Flight Model 2 was eliminated by a design modification which had been made earlier for reasons relating to noise immunity. In a satellite program the prospective experimenter must be expected to deal with such occurrences many times. Of course, it is also true that technological improvement may simplify the system design. Equipment, however, should be designed with the objective of taking advantage of innovations.

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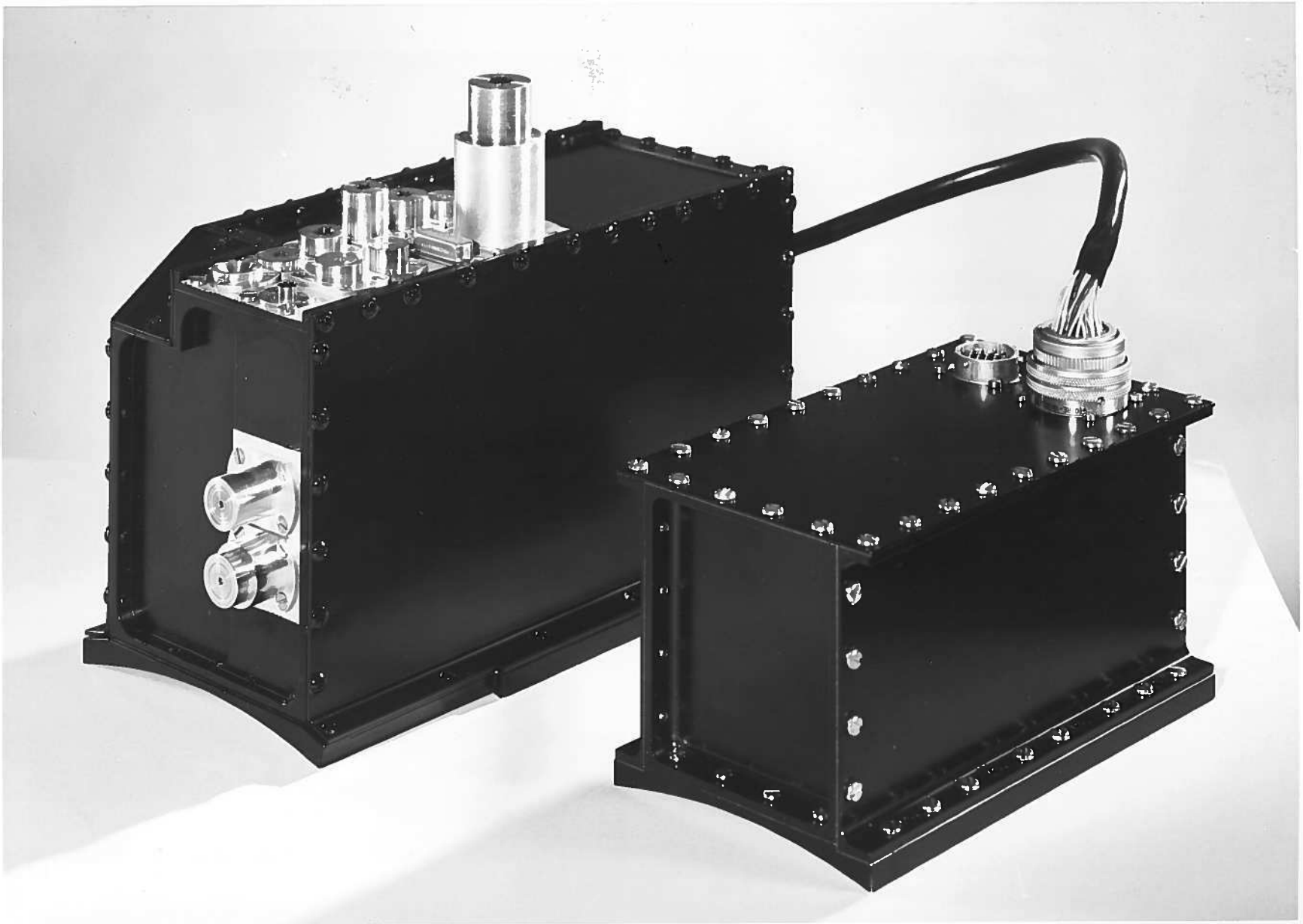


Plate I EPD experiment showing detector and encoder packages

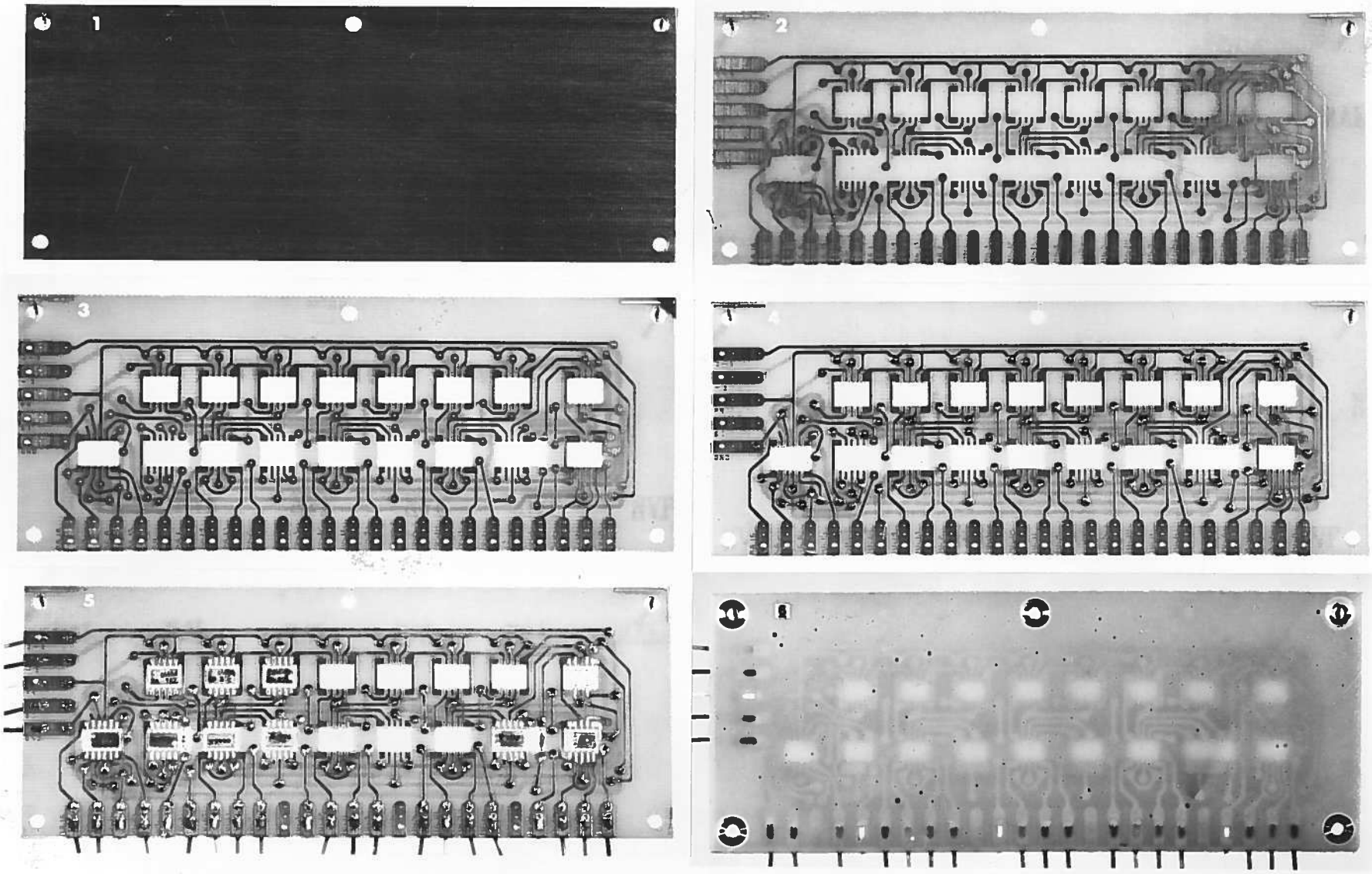


Plate II Six stages in fabrication of typical encoder wafer

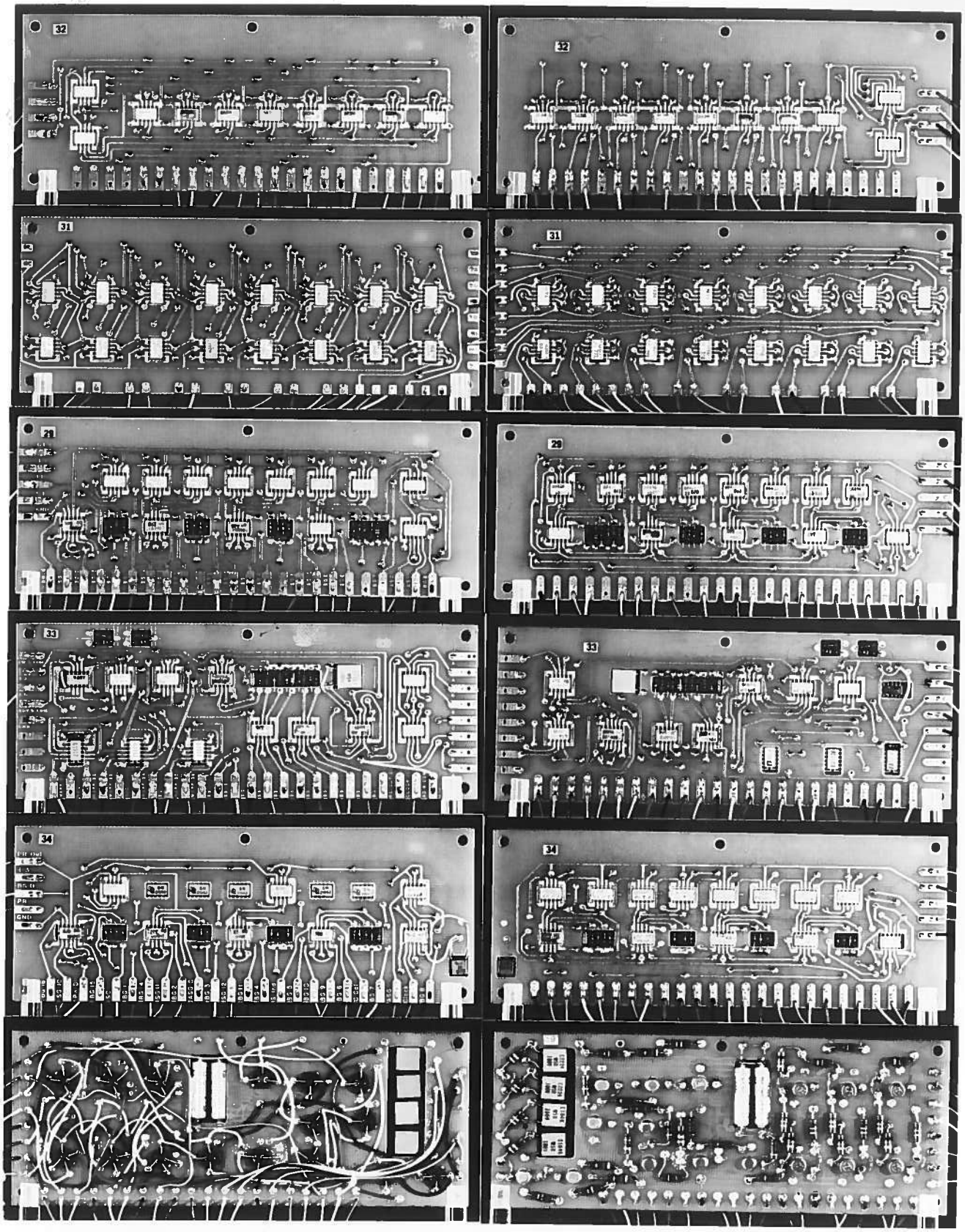


Plate III Top and bottom views of board types in Engineering and Flight Model 1

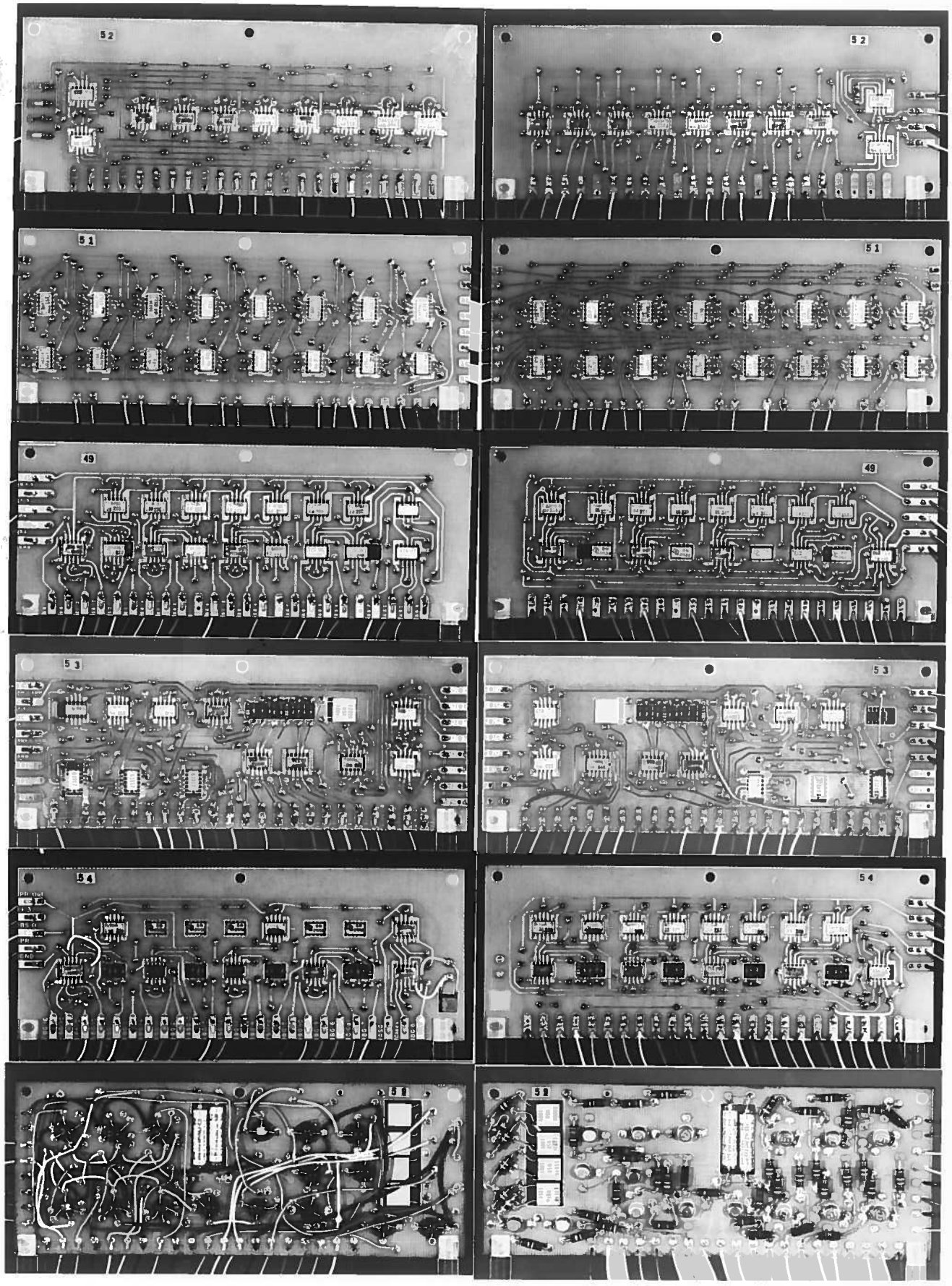
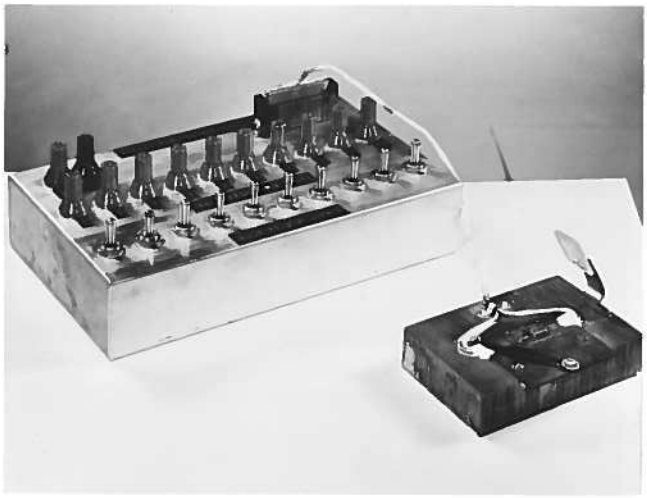
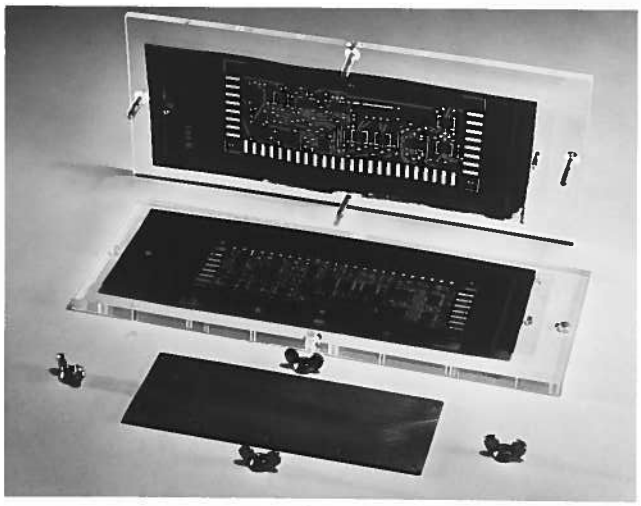


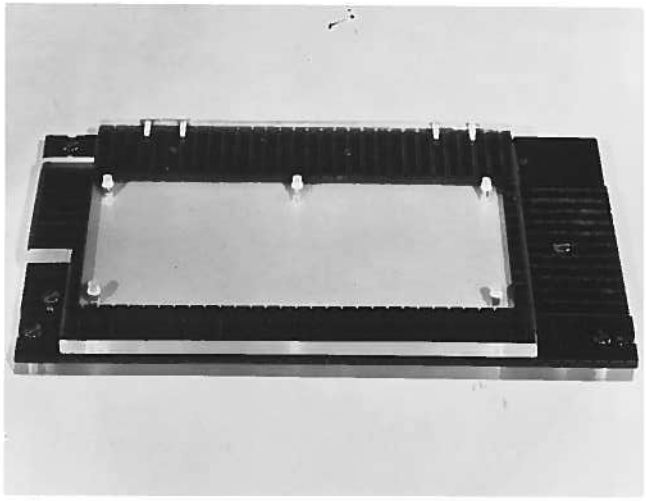
Plate IV Top and bottom views of board types in Flight Model 2



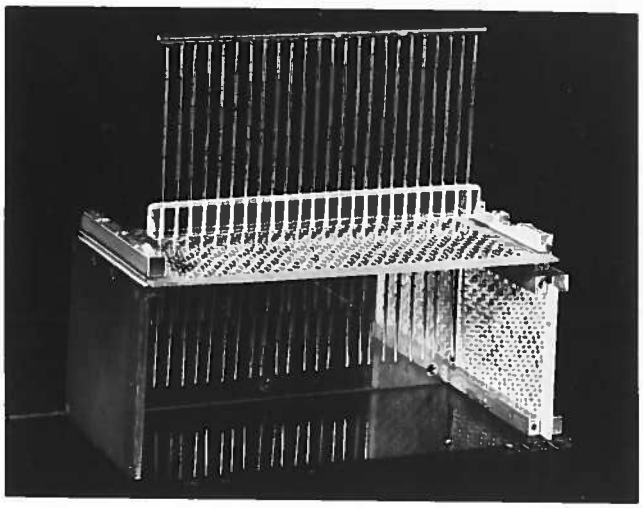
IC Test Jig



Photographic Jig



Potting Mould



Comb

Plate V Encoder construction jigs

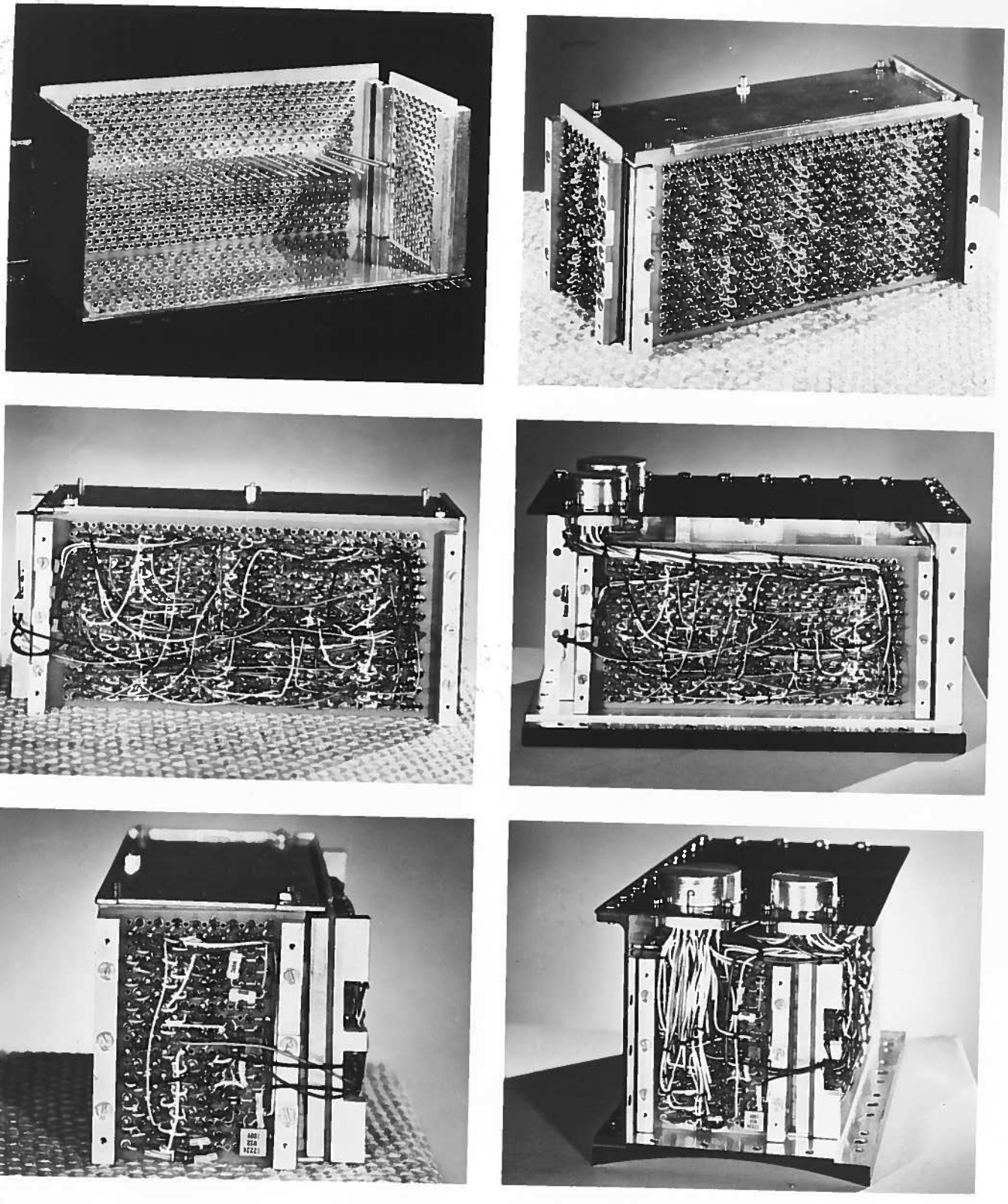


Plate VI Encoder assembly views