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GaN HEMT and MOS monolithic integration on silicon substrates

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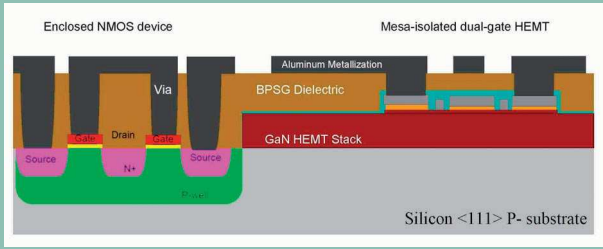
A process for monolithically integrating MOS and AlGaN/GaN HFETs has been developed using a windowed epitaxy technique. AlGaN/GaN HFET devices display a forward current greater than 0.8 A/mm and a breakdown voltage larger than 200 V. Field-plated devices have also been demonstrated. Enclosed MOS devices based on a 900°C thermal oxide have been produced showing promising characteristics.



Cross section schematic of integrated devices

1 Introduction Gallium nitride HEMT devices are ideal for high-power operation due to their high mobility and large breakdown voltage as a result of the large bandgap of the material (3.4 eV) [1]. Currently, the applications for AlGaN/GaN HEMT devices are limited to RF and microwave power transistors, as well as some preliminary power switching applications, due to the restrictive cost of growth compared to silicon-based alternatives. The development of growth on silicon substrates allows for a cheaper alternative than the current norm of silicon carbide substrates [2, 3].

The growth of AlGaN/GaN on Si also opens the path to the integration of high-density, low-power MOS logic with high power HEMTs, expanding the number of applications for which GaN can be competitive. Applications that can take advantage of this could include high-power switching circuits that use MOS logic for control, or chemical/biological sensors which can take advantage the chemical inertness of the AlGaN/GaN material structure for detection, combined with low-power MOS read-out circuitry.

This work reports on the monolithic integration of AlGaN/GaN HEMTS and MOS technology on silicon <111> substrates using a windowed epitaxy technique. A co-integration process which first includes the high-temperature MOS processing steps, followed by the GaN device formation is presented. Improved measured MOS and HFET IV characteristics compared to those previously reported are presented [4]. Integration of Si MOS and AlGaN/GaN HEMT devices has also been reported by Chung *et al.* [5] using a wafer bonding technique. This allows for the use of <100> oriented substrates, currently preferred for MOS devices.

2 Substrate preparation and growth The windowed growth process on silicon <111> substrates presented in [6] is used to prepare wafers with dedicated regions for MOS and GaN devices. This technique uses a silicon dioxide layer to protect regions of the silicon wafer for MOS processing during GaN epitaxy. This layer is subsequently lifted off using a HF wet etch after growth,

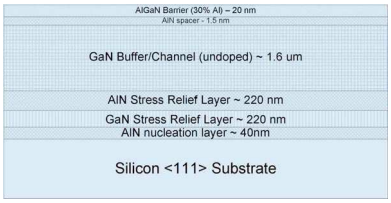


Figure 1 GaN HEMT epitaxial structure grown by ammonia-MBE

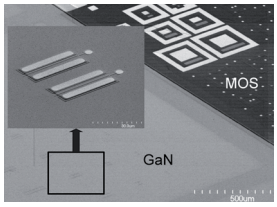


Figure 2 SEM image of integrated GaN HFET and MOS enclosed devices before metallization steps

re-exposing regions of atomically smooth silicon located adjacent to the GaN heterostructure.

The GaN heterostructure is grown by ammonia-MBE between 780 °C and 900 °C with a NH_3 flow of 200 sccm. The layer stack, which is shown in Fig. 1, uses the stress relief strategy developed in [2] in order to overcome the lattice and thermal expansion mismatch between GaN and silicon. It should be noted that the sample used in this work has an unintentionally doped buffer layer rather than using carbon doping. The growth results in mobility of 917 cm^2/Vs, a sheet resistance of 445 Ω/sq and a sheet carrier concentration of $1.07x10^{13}$ cm^{-2}. Additionally, this sample is able to withstand long thermal cycles at temperatures greater than 950 °C when passivated with a thin oxide capping layer. Previous growths have shown some decomposition of the material under these conditions.

3 Device processing The limited thermal budget of the MOS process is the most challenging requirement of the co-integration process, as above 950 °C, the GaN material can begin to decompose. To ensure that the material survives MOS processing, the maximum temperature used for oxidations is 900 °C. Additionally, only enclosed devices are used in this process to avoid the long high-temperature oxidation steps needed for device isolation with thick thermally grown field oxide, since shallow trench isolation was not available here. A schematic cross-section through the completed devices is shown as the title figure.

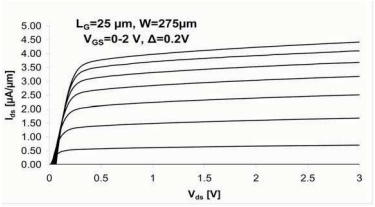
MOS fabrication must be done prior to HEMT processing, as the high temperature steps required for MOS will degrade both ohmic and Schottky metallization of HEMT devices. A thermal CVD oxide is used to protect the AlGaN/GaN surface during these steps, which begin with a three-implant $^{11}B^+$ retrograde well formation used in order to eliminate long thermal diffusions. Next, a 25 nm thermal gate oxidation is performed at 900 °C in a dry O_2 ambient, followed by a 30 minute inert ambient anneal. Polysilicon LPCVD gates are then deposited at 625 °C and dry etched. Source/drain diffusions are performed using a $POCl_3$ source at 900 °C for 30 minutes, resulting in a sheet resistance of 33 Ω/sq. A borophosphosilicate (BPSG) glass is then deposited and flowed to protect the MOS regions during HEMT fabrication.

GaN device fabrication begins with mesa formation using chemically-assisted ion-beam etching (CAIBE). A Ti/Al/Ti/Al ohmic contact structure is then used after an HCl pre-treatment to remove the native oxide formed on the AlGaN. The ohmic metal is subsequently annealed at 855 °C for 60 seconds in a nitrogen ambient. This anneal does not affect MOS performance as the devices have not been metallized at this point, and are buried in BPSG. An Au-based ohmic contact is not an option, as it is not compatible with MOS fabrication. A Pt-based schottky gate is then deposited using e-beam evaporation. Devices are subsequently passivated with a thin SiN layer used to mitigate the effects of current collapse. RIE plasma etching with a CF_4/O_2 chemistry is used to open via holes in both the SiN passivation in the GaN region, and the BPSG in the MOS region prior to a joint aluminum co-metallization to finish the process. A SEM image of the sample before final metallization is shown in Fig. 2.

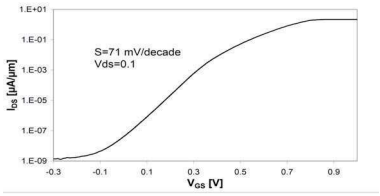
4 MOSFET performance The forward drain current and subthreshold characteristics for the enclosed MOS devices are shown in Fig. 3. The MOS devices have a threshold voltage of 0.35 V, which is close to that predicted by TSuprem4 simulation. The subthreshold swing is 70.4 mV/decade, demonstrating strong gate control of channel charge. The contact resistance of the MOS devices is $1.68x10^{-5}$ Ωcm^2.

The MOS devices demonstrated some gate leakage, which can be explained by the orientation of the substrate as well as the low gate oxidation temperature due to the limited thermal budget [7,8]. Modern MOS processes, which have moved away from using thermal oxidation, have lower thermal budgets, and should therefore be more compatible for GaN integration. Additionally, growth on silicon <110> oriented substrates has been demonstrated [3]. These substrates are of increasing interest for MOS devices due to a larger hole mobility.

5 HFET performance Both field-plated and non-field-plated dual-gate HEMTs were fabricated on this wafer, with gate widths ranging from 10 µm to 320 µm and a fixed gate length of 0.8 µm. Figure 4 shows the DC performance of a dual-gate GaN HEMT device with a gate length of 0.8 µm and total width of 80 µm. The forward drain current of standard devices exceeded 0.81 A/mm, higher than values reported in previous work due to im-

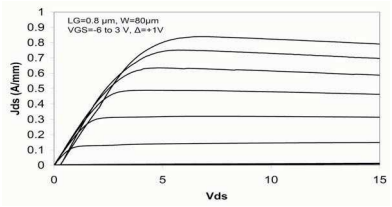


a) Forward current: I_{DS} vs. V_{DS}

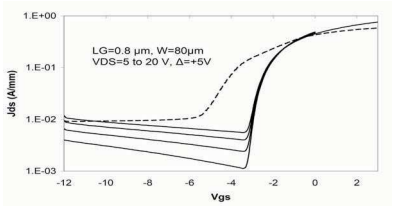


b) Subthreshold: I_{DS} vs. V_{GS}

Figure 3 MOS DC characteristics of enclosed NMOS device



a) Forward Current: I_{DS} vs V_{DS}



b) Gate Leakage: J_{GS} vs V_{GS}

Figure 4 DC measurements for dual-gate AlGaN/GaN HEMT

Table 1 Breakdown Voltage vs Gate-Drain Spacing

Gate-Drain Spacing	Breakdown Voltage
2.2 µm	54 V
3.2 µm	93 V
4.2 µm	140 V
5.2 µm	>200 V

proved metallization and ohmic contacts. The pinch-off voltage is approximately -3.3 V. Corbino structures were used to measure a sheet resistance of 445 Ω/sq and specific contact resistance of 4.4x10^{-5} Ωcm^2 for the Ti/Al/Ti/Al ohmic metal.

The lack of Carbon doping in the buffer layer compared to that of previous work is the most probable cause of the rising leakage current as the gate becomes highly reverse biased. Carbon-doped devices shown in previous work demonstrate a flat subthreshold curve as shown by the dashed line in Fig. 4b [4].

The breakdown voltage of the devices also ranged from 53 V for a 2.2 µm gate-drain spacing to greater than 200 V for a 5.2 µm gate-drain spacing. Devices were pinched off with a gate voltage of -8 V while the drain voltage was increased. Breakdown was observed by monitoring the gate current, as this increases sharply at the onset of breakdown. Table 1 demonstrates this trend correlating the gate-drain spacing to the breakdown voltage as shown in [9]. These high breakdown voltages on non-optimized devices demonstrate the potential of HEMT integration to greatly increase the voltage-handling capability of MOS.

6 Conclusion Enclosed silicon MOS devices have been monolithically integrated with high performance dual-gate AlGaN/GaN HEMTs on silicon <111> substrates. A windowed epitaxy technique is the key to preserving a suitable surface on which to fabricate MOS devices. This epitaxy technique is also easily scaled up to larger wafer sizes that allows for commercial-scale production. The performance of both MOS and GaN devices is improved over previous work due to improved metallization schemes and minor process adjustments. The MOS would exhibit better performance with a larger thermal budget. However only a limited thermal budget can be used for the GaN layers to survive MOS processing. With state-of-the-art MOS fabrication, much lower temperatures are needed to produce fully functioning devices. The topological difference between the GaN and Si could present some process complications in lithography, and oxide backfill for metallization. Using this integration technique with modern MOS processing should result in optimal performance of both technologies. Additionally, work is underway to transfer this integration to more industrially-relevant silicon <110> substrates.

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